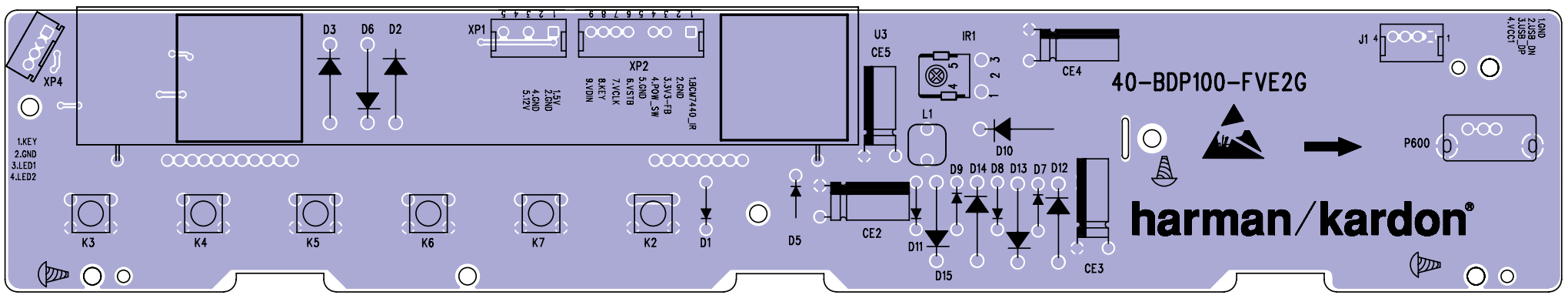
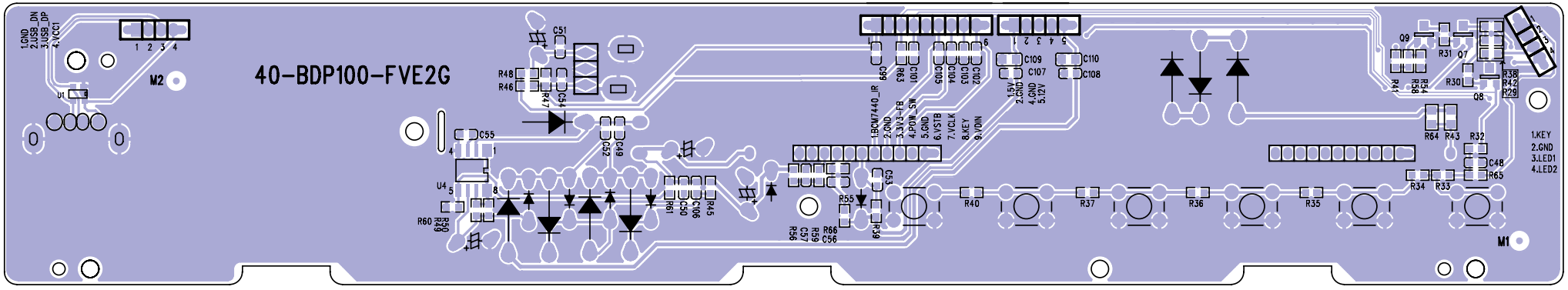
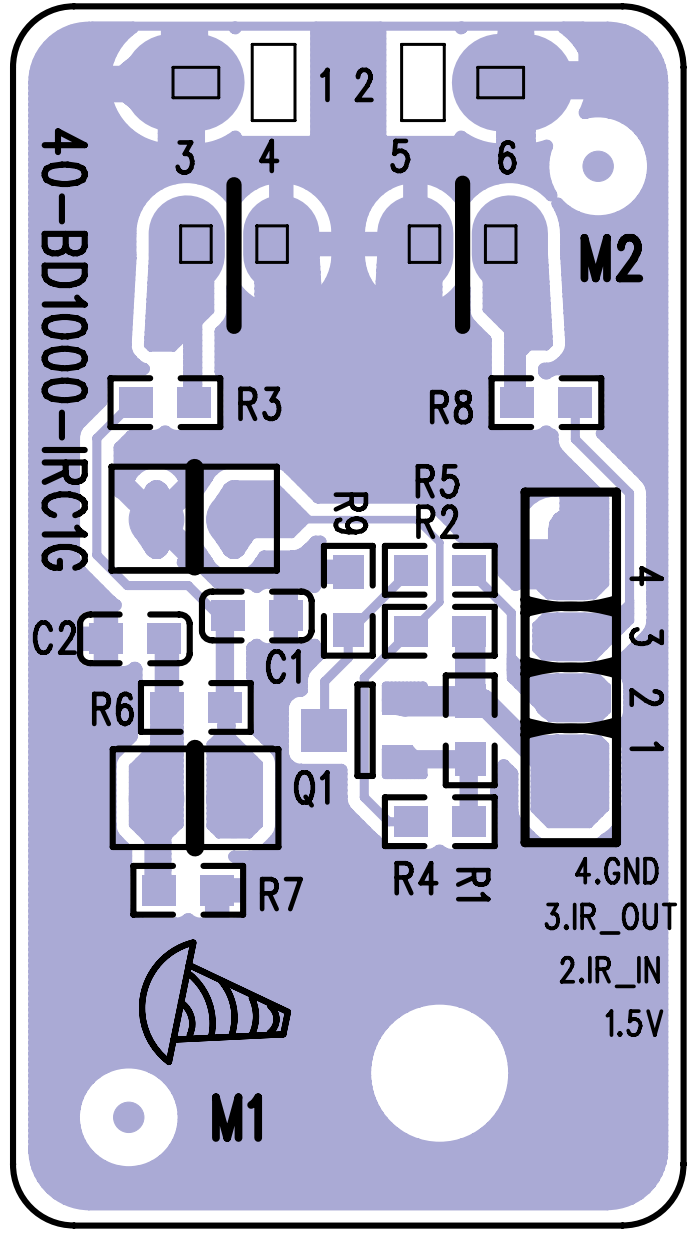
Front Board Print-layout (Top side):



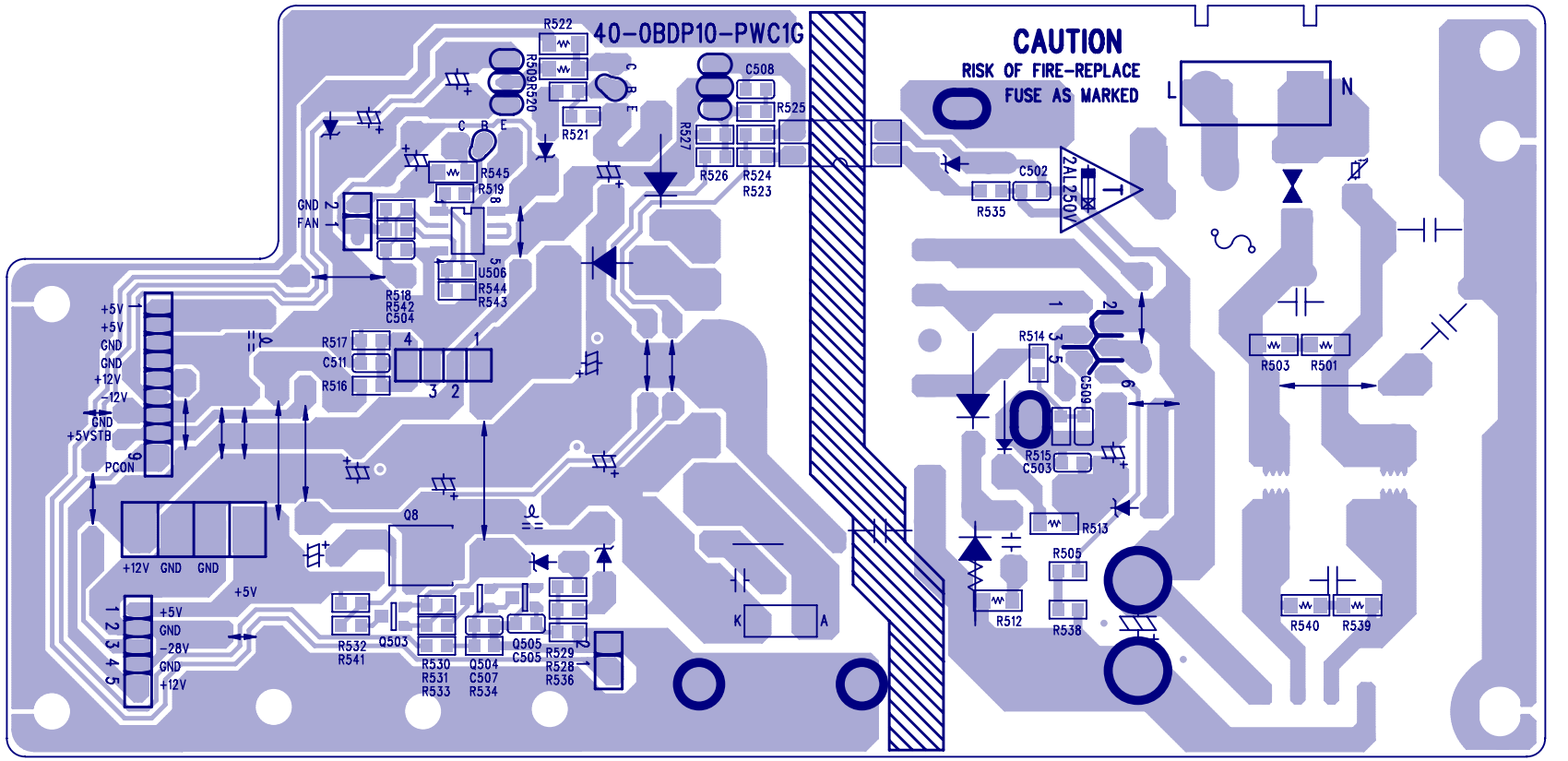
Front Board Print-layout (Bottom side):



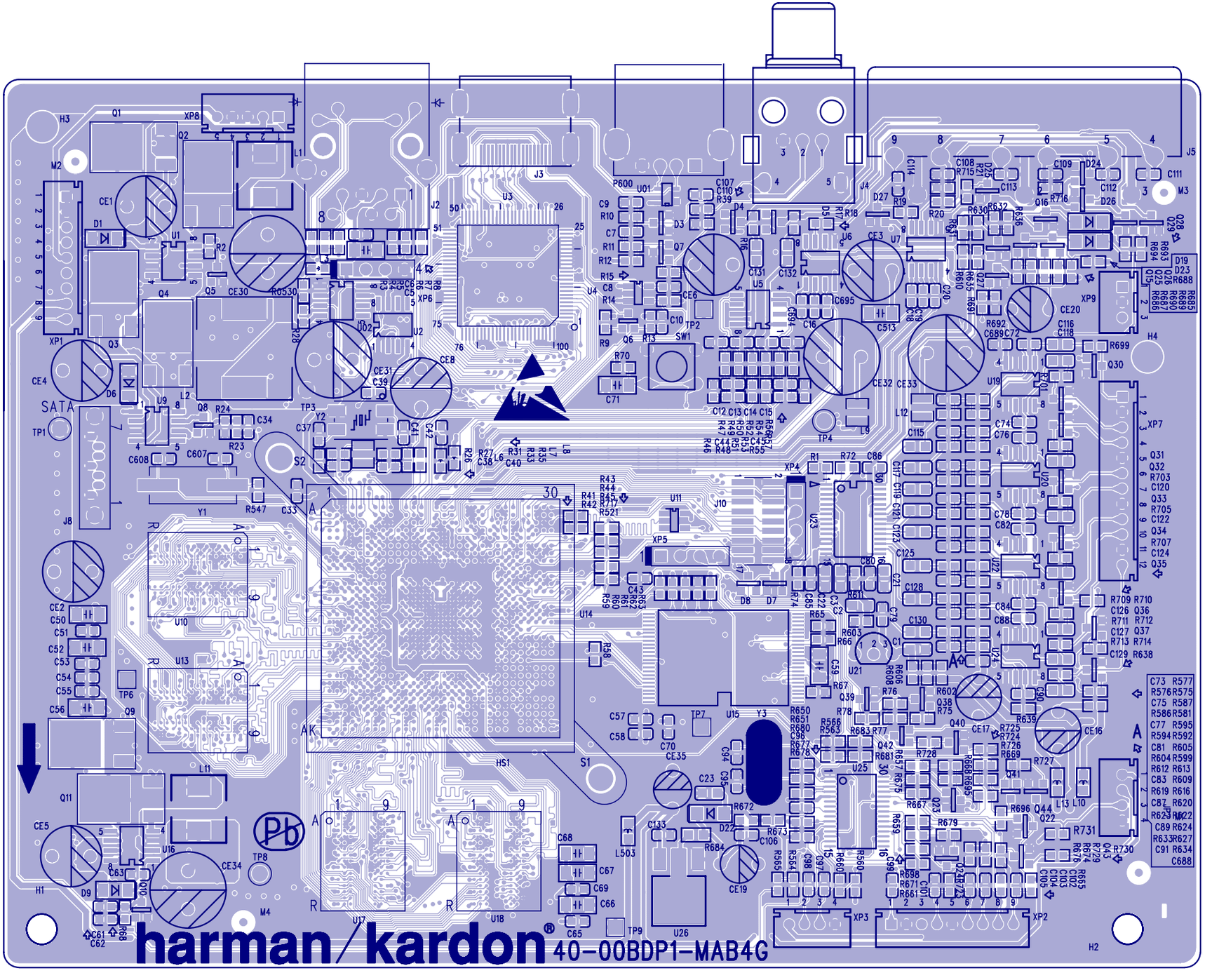
IR Board Print-layout (Bottom side):



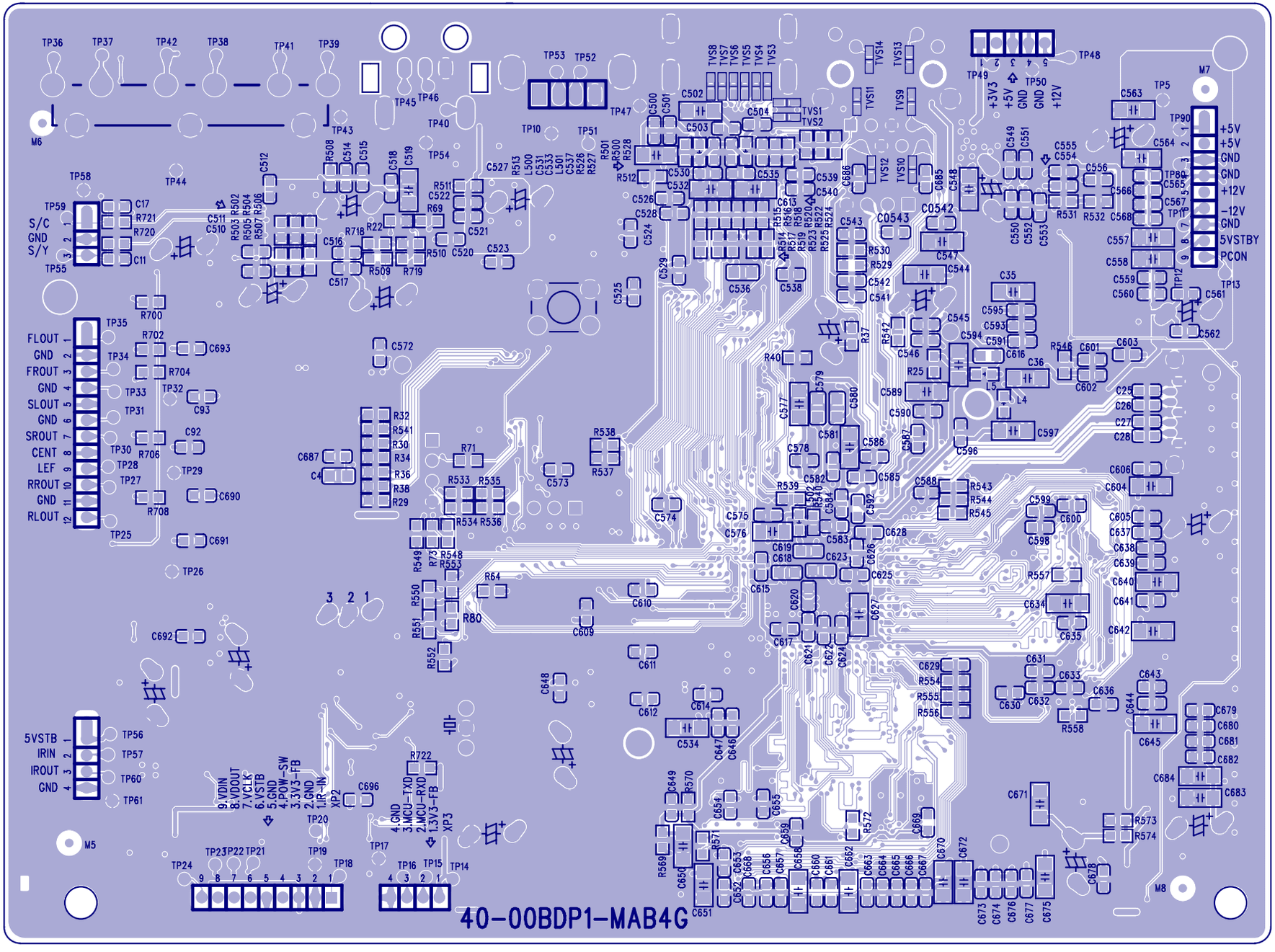
Power Board Print-layout (Bottom side):



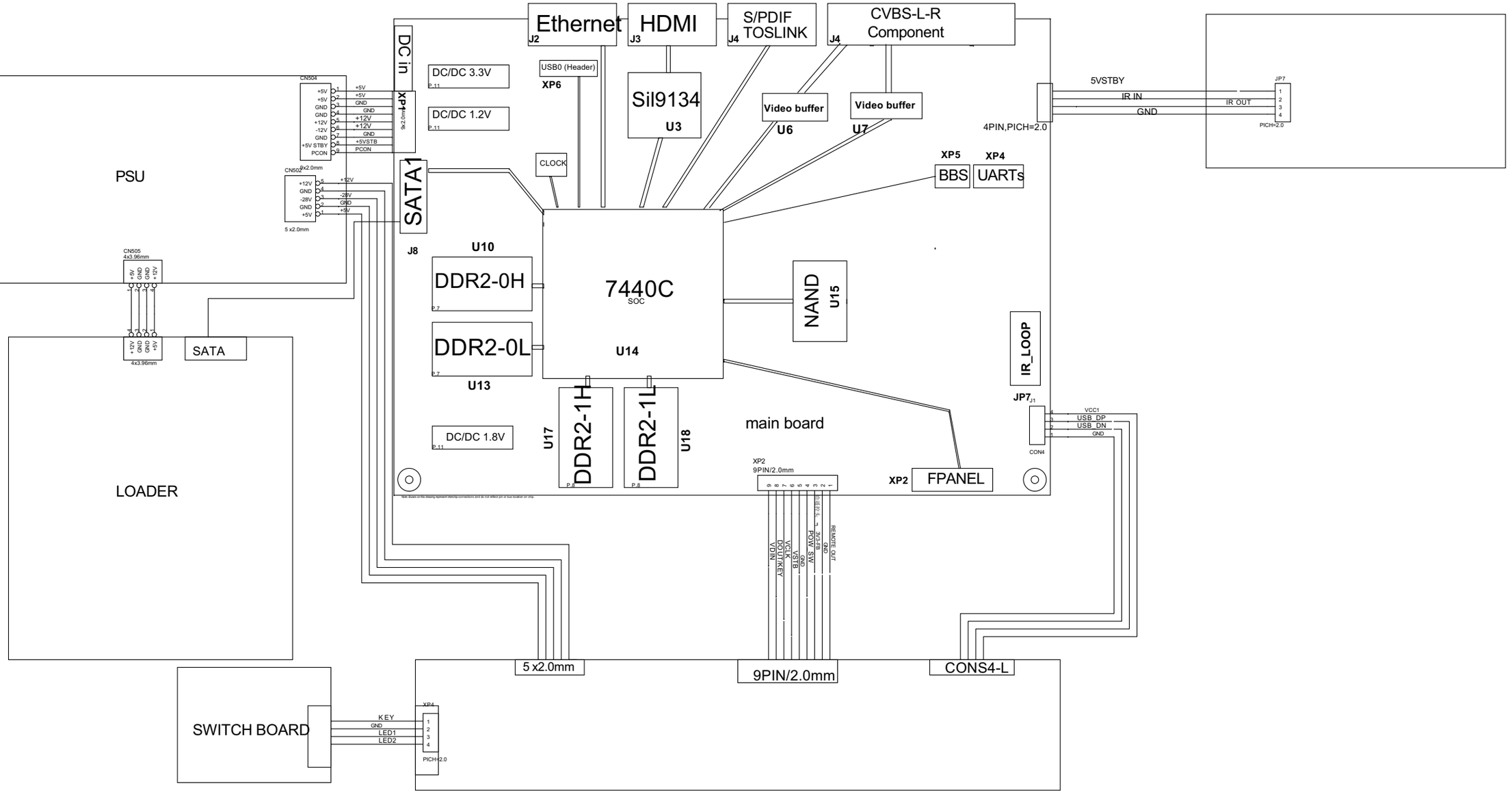
Main Board Print-layout (Top side):



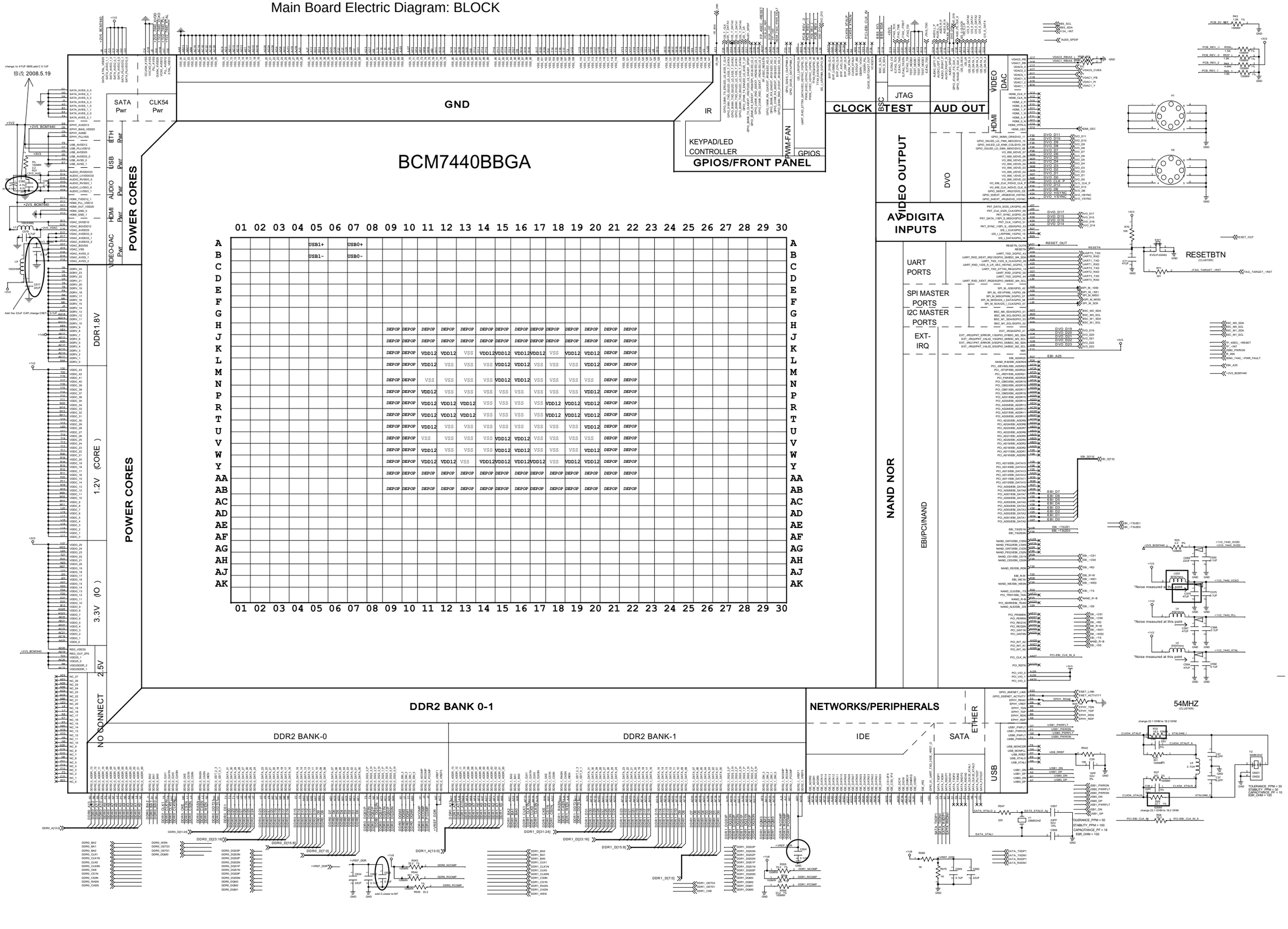
Main Board Print-layout (Bottom side):



Harman BDP 10/BDP 1 Block Diagram

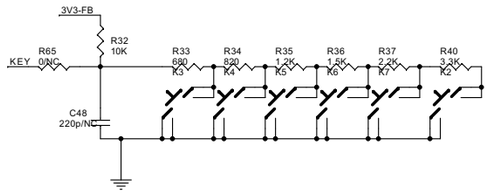


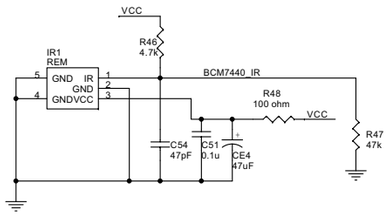
Main Board Electric Diagram: BLOCK

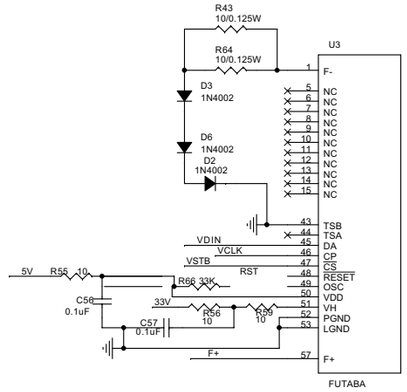


7-1

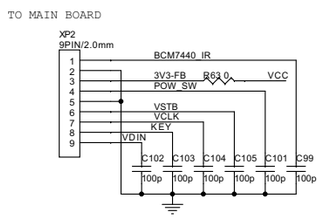
Front Board Electric Diagram: MCU+VFD(FUTABA)

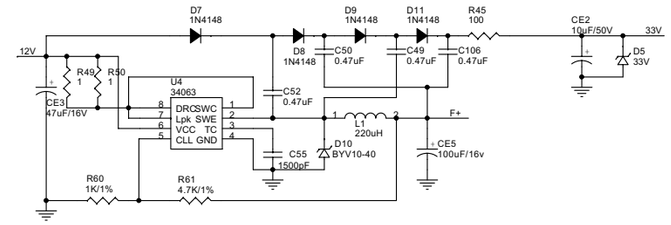


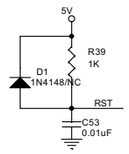


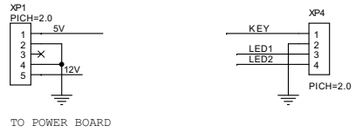


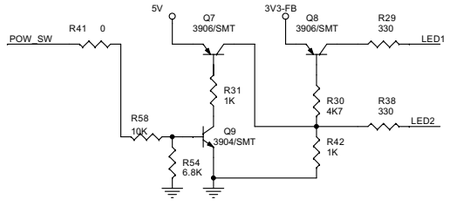
TO MAIN BOARD

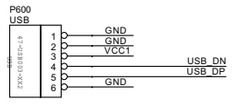


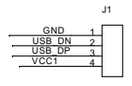


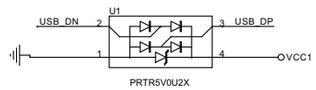






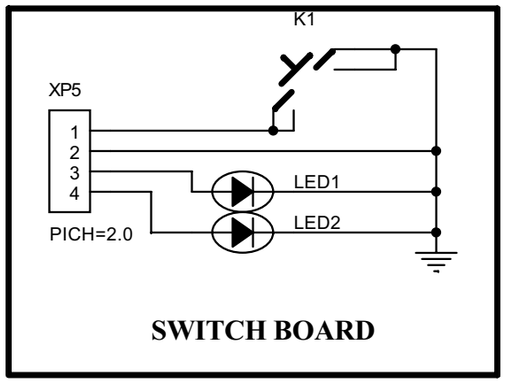






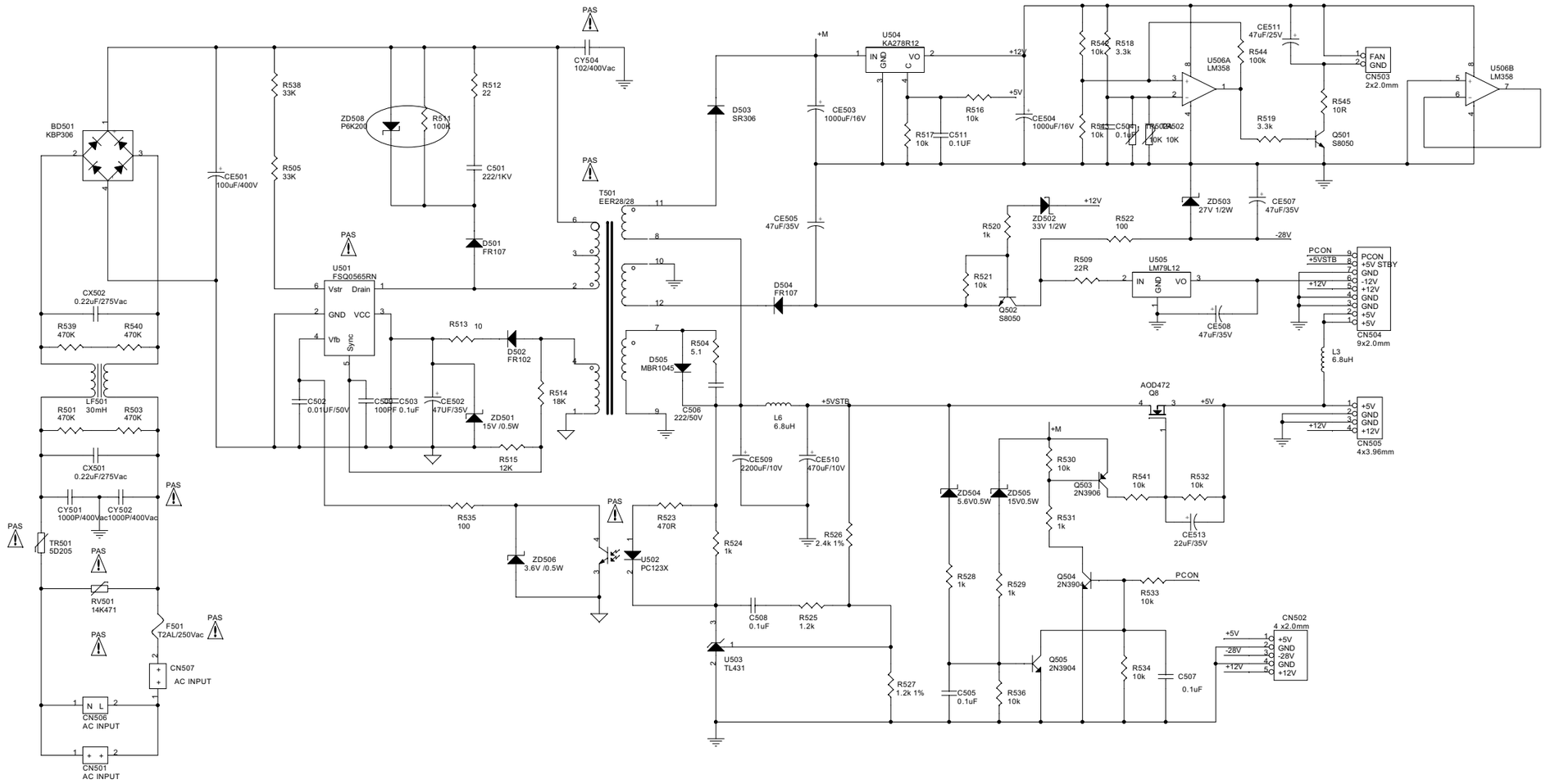
7-2

Switch Board Electric Diagram:



7-3

Power Board Electric Diagram:



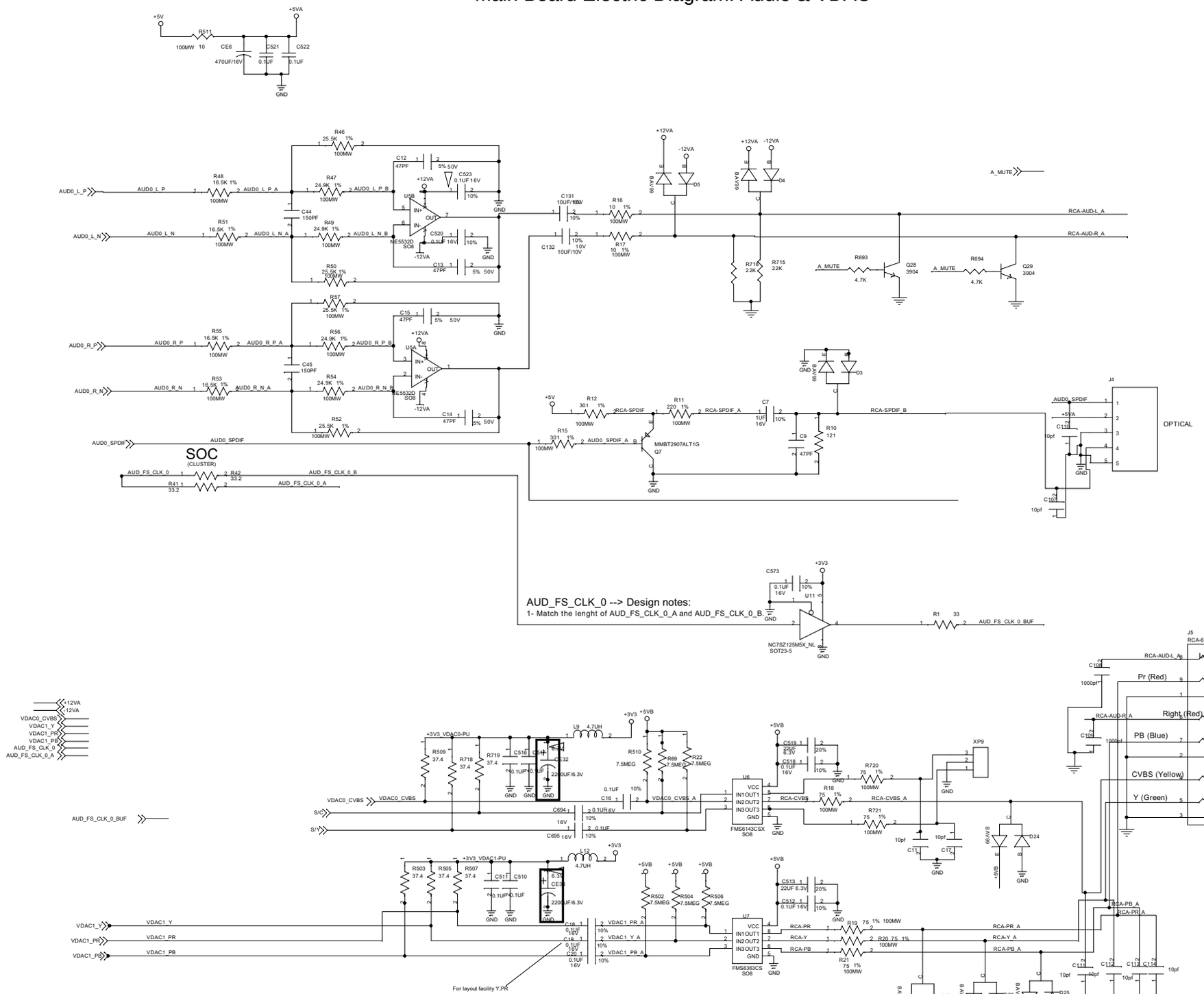
*** CAUTION :**

THE PARTS MARKED WITH PAS ARE IMPORTANT PARTS ON THE SAFETY.

PLEASE USE THE PARTS HAVING THE DESIGNATED PARTS NUMBER WITHOUT FAIL.

Audio & VDAC

Main Board Electric Diagram: Audio & VDAC

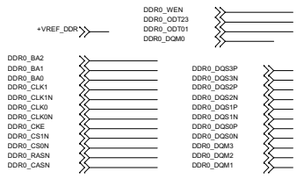


VIDEO ANALOG --> Design notes and Layout Guidelines:

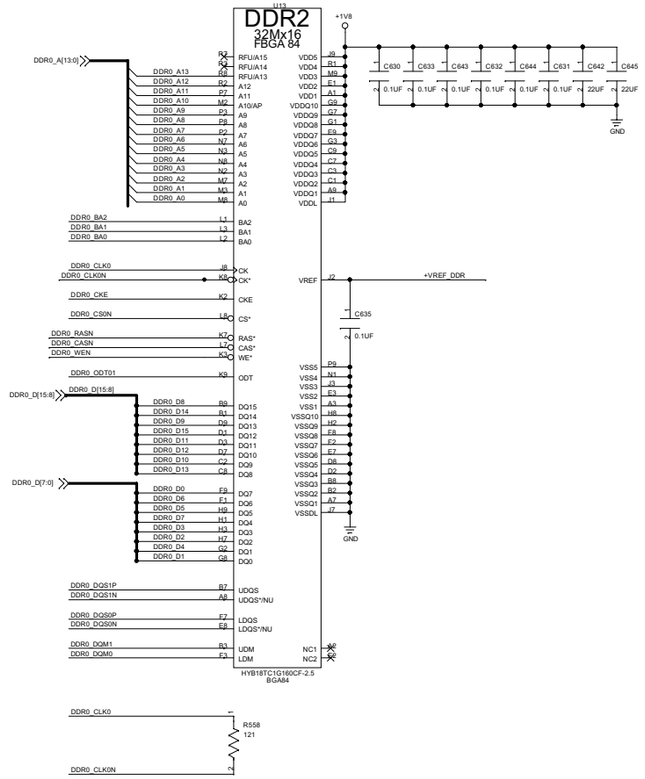
1- The Fairchild active filter are EDS protected.
2- The Fairchild active filter and terminations must be place close to video connectors.
3- Analog video outputs are sensitive to noise coming from the power. Beads and inductors must be consider to clean the noise. Try to keep a good noise immunity of your power traces and plane areas into the video output PCB area.
4- 37.4 Ohms resistors terminate the lines between BCM7440 and the active filters. They also polarize the 7440 VDAC outputs. They 3.3V used for these pull-up must be very clean.
5- VDAC outputs traces must be routed according to the isolated traces rule. Trace_to_trace clearance >= 10 mils.
6- Place VDAC0/1_RBIAS resistors very very close to their BCM7440 pins (trace lenght <= 100mils).

DDR2 BANK-0

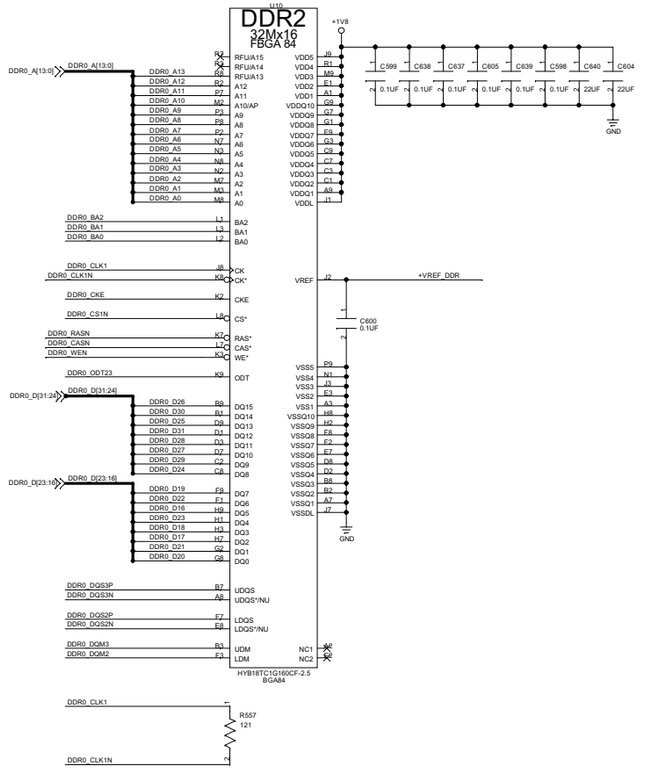
Main Board Electric Diagram:DDR2 BANK-0



DDR2-0L
(CLUSTER)



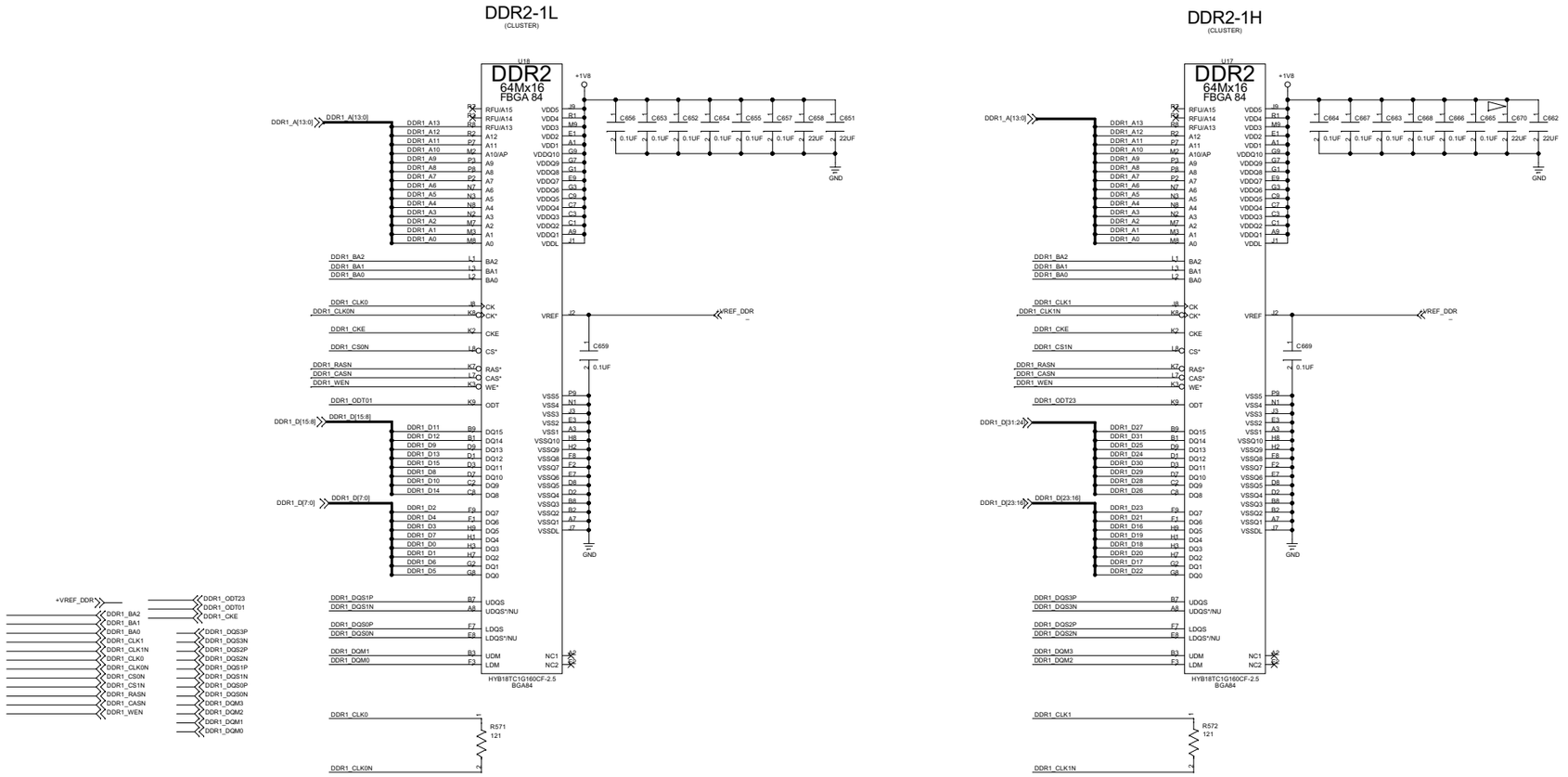
DDR2-0H
(CLUSTER)



BCM7440 DDR2 2x16 --> Design notes and Layout Guidelines:
1- Place 121 ohms clock termination at the end of the differencial trace.
2- Pin swaping can only be done on data lines inside each group of 8 bit (Byte Lane).
3- Length of all Data signals into a Byte Lane should be matched together (<100 mils).
4- Length of all Data signals between Byte Lane should be matched together (<400 mils).
5- DDR2 clock and DQS P/N traces must be routed as 100 Ohms Differential pairs. Traces width and gap according to PCB stackup.
6- When developing the PCB floor plan, the proximity of the DDR2 device to the memory controller is an important factor.
- To avoid the use of external address termination on high-speed DDR2, the address trace length should be less than 2.5in.
* If those requirements can not be reached, refer to JEDEC JESD79-2B standard for design rules and terminations.

DDR2 BANK-1

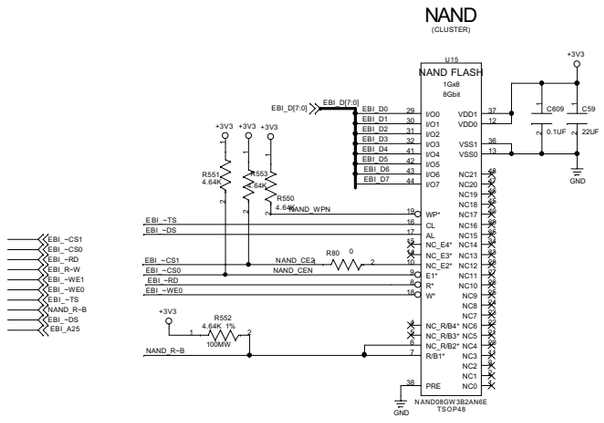
Main Board Electric Diagram: DDR2 BANK-1



BCM7440 DDR2 2x16 --> Design notes and Layout Guidelines:
1- Place 121 ohms clock termination at the end of the differencial trace.
2- Pin swaping can only be done on data lines inside each group of 8 bit (Byte Lane).
3- Length of all Data signals into a Byte Lane should be matched together (<100 mils).
4- Length of all Data signals between Byte Lane should be matched together (<400 mils).
5- DDR2 clock and DQS P/N traces must be routed as 100 Ohms Differential pairs. Traces width and gap according to PCB stackup.
6- When developing the PCB floor plan, the proximity of the DDR2 device to the memory controller is an important factor.
- To avoid the use of external address termination on high-speed DDR2, the address trace length should be less than 2.5in.
* If those requirements can not be reached, refer to JEDEC JESD79-2B standard for design rules and terminations.

NAND

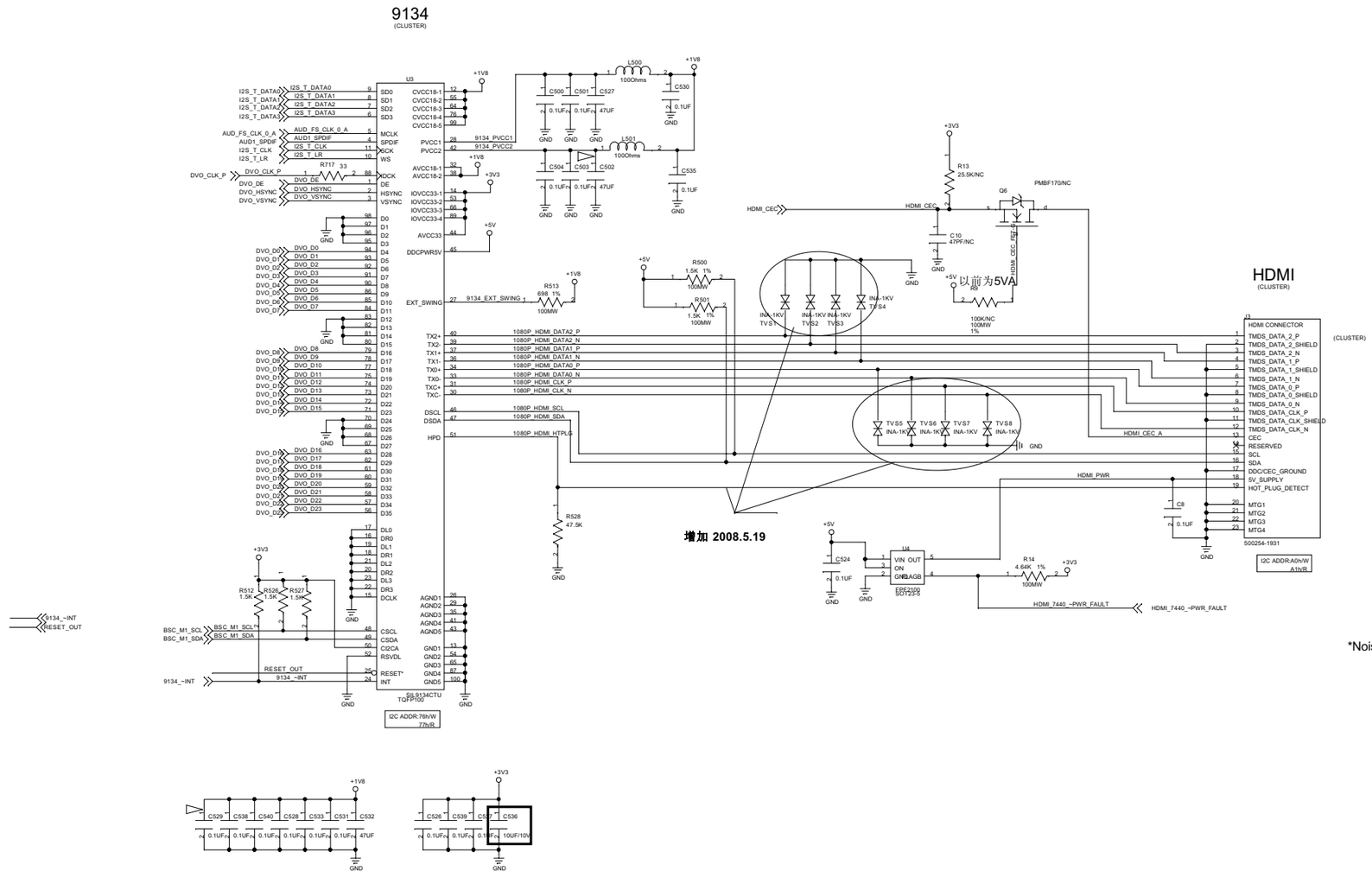
Main Board Electric Diagram: NAND



EBI	NAND	PCI
EBI_ADDR25	-------	-------
EBI_ADDR24	-------	-------
EBI_ADDR15	-------	PCI_AD31
EBI_ADDR14	-------	PCI_AD30
EBI_ADDR13	-------	PCI_AD29
EBI_ADDR12	-------	PCI_AD28
EBI_ADDR11	-------	PCI_AD27
EBI_ADDR10	-------	PCI_AD26
EBI_ADDR9	-------	PCI_AD25
EBI_ADDR8	-------	PCI_AD24
EBI_ADDR7	-------	PCI_AD23
EBI_ADDR6	-------	PCI_AD22
EBI_ADDR5	-------	PCI_AD21
EBI_ADDR4	-------	PCI_AD20
EBI_ADDR3	-------	PCI_AD19
EBI_ADDR2	-------	PCI_AD18
EBI_ADDR1	-------	PCI_AD17
EBI_ADDR0	-------	PCI_AD16
EBI_DATA15	-------	PCI_AD15
EBI_DATA14	-------	PCI_AD14
EBI_DATA13	-------	PCI_AD13
EBI_DATA12	-------	PCI_AD12
EBI_DATA11	-------	PCI_AD11
EBI_DATA10	-------	PCI_AD10
EBI_DATA9	-------	PCI_AD9
EBI_DATA8	-------	PCI_AD8
EBI_DATA7	NAND_I/O7	PCI_AD7
EBI_DATA6	NAND_I/O6	PCI_AD6
EBI_DATA5	NAND_I/O5	PCI_AD5
EBI_DATA4	NAND_I/O4	PCI_AD4
EBI_DATA3	NAND_I/O3	PCI_AD3
EBI_DATA2	NAND_I/O2	PCI_AD2
EBI_DATA1	NAND_I/O1	PCI_AD1
EBI_DATA0	NAND_I/O0	PCI_AD0
EBI_ADDR19	-------	PCI_~CBE03
EBI_ADDR18	-------	PCI_~CBE02
EBI_ADDR17	-------	PCI_~CBE01
EBI_ADDR16	-------	PCI_~CBE00
EBI_ADDR20	-------	PCI_PAR
-------	-------	PCI_~FRAME
EBI_~TA	-------	PCI_~TDRY
EBI_ADDR21	-------	PCI_~IRDY
EBI_ADDR22	-------	PCI_~STOP
EBI_ADDR23	-------	PCI_~DEVSEL
EBI_~TEA	-------	PCI_~SERR
-------	-------	PCI_~PERR
EBI_~CS2	-------	PCI_~REQ3
EBI_~CS4	-------	PCI_~REQ2
-------	-------	PCI_~REQ1
-------	-------	PCI_~REQ0
EBI_~CS3	-------	PCI_~GNT3
EBI_~CS5	-------	PCI_~GNT2
-------	-------	PCI_~GNT1
-------	-------	PCI_~GNT0
-------	-------	PCI_CLK_IN
-------	-------	PCI_~RST
-------	-------	PCI_INT_A2
-------	-------	PCI_INT_A1
-------	-------	PCI_INT_A0
EBI_~CS1	NAND_CE1	-------
EBI_~CS0	NAND_CE0	-------
EBI_~RD	NAND_RE	-------
EBI_~WE1	-------	-------
EBI_~WE0	NAND_WE	-------
EBI_~TSIZE1	-------	-------
EBI_~TSIZE0	-------	-------
EBI_~TS	NAND_CLE	-------
EBI_~TA2	NAND_R~B	-------
EBI_~DS	NAND_ALE	-------
EBI_R~W	-------	-------

DVO, SIL9134, HDMI

Main Board Electric Diagram: DVO, SIL9134, HDMI



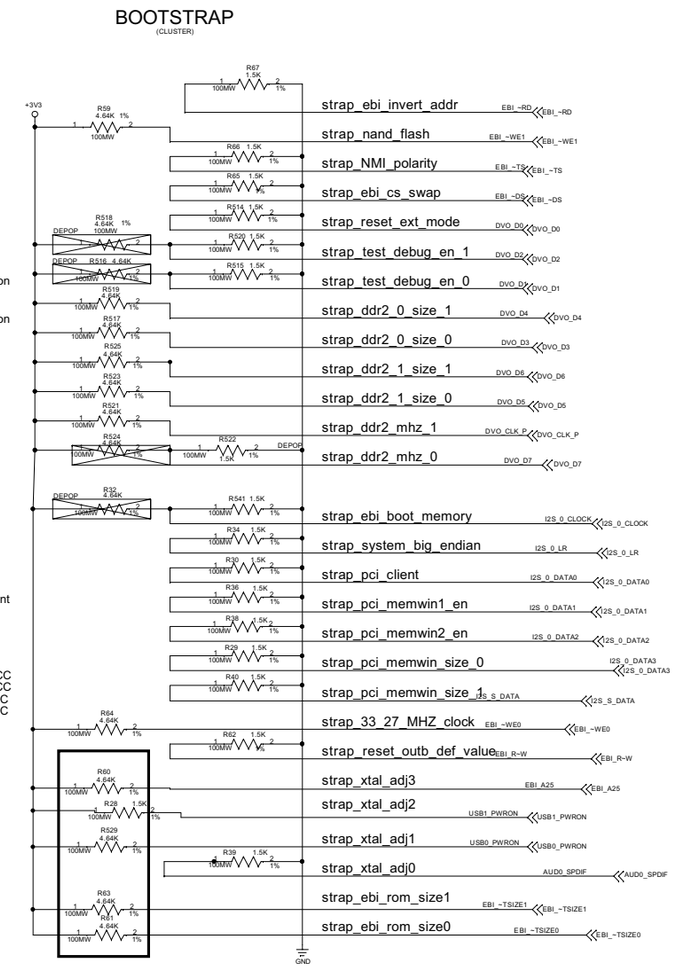
HDMI --> Design notes and Layout Guidelines:

1- HDMI Data and clockP/N traces must be routed as 100 Ohms Differential pairs. Traces width and gap according to PCB stackup.
2- Match trace lenght of P/N differential pairs. 20 mils max within a pair and 100 mils max between pairs.
3- Route differential pairs above the GND plane. Do not split the GND plane under differential pairs.
4- Use minimum number of VIA.
5- When possible, use higher clearance distance between differantials pairs and any others traces (>15 mils).
6- If higher than 2KV protection is necessary on HDMI port use low capacitance ESD protections close to the HDMI connector.
7- Consider limiting current to Maximum 500mA on HDMI 5V power.

Main Board Electric Diagram: BOOT STRAP OPTIONS & BCM7440B

Boot Strap Options

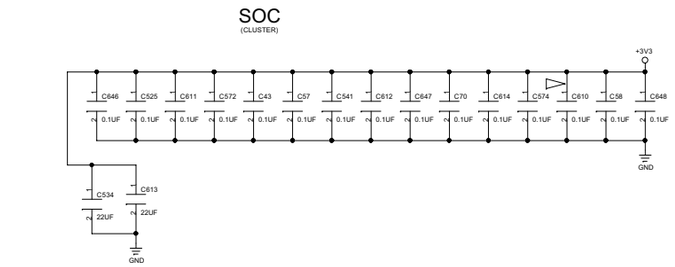
0	strap_ebi_invert_addr	1: Invert upper bits of EBI address 0: Do not invert EBI address
1	strap_nand_flash	1: External NAND FLASH present 0: External NOR FLASH present
0	strap_NMI_polarity	1: High-active interrupt 0: Low-active interrupt
0	strap_ebi_cs_swap	1: Swap CS_0 and CS_1 signals 0: No swap
0	strap_reset_ext_mode	
0	strap_test_debug_en_1	
0	strap_test_debug_en_0	
1	strap_ddr2_0_size_1	3: DDR2 Controller Manual Initialization 2: DDR2 bank 0 size = 256/512 MB
1	strap_ddr2_0_size_0	1: DDR2 bank 0 size = 128 MB 0: DDR2 bank 0 size = 64 MB
1	strap_ddr2_1_size_1	3: DDR2 Controller Manual Initialization 2: DDR2 bank 0 size = 256/512 MB
1	strap_ddr2_1_size_0	1: DDR2 bank 0 size = 128 MB 0: DDR2 bank 0 size = 64 MB
1	strap_ddr2_mhz_1	3: DDR2 Banks = 400/800 MHZ 2: DDR2 Banks = 333/667 MHZ
1	strap_ddr2_mhz_0	1: DDR2 Banks = 266/533 MHZ 0: DDR2 Banks = 200/400 MHZ
0	strap_spi_slave_enable	1: SPI slave port configured 0: BSC slave port configured Fix.
0	strap_ebi_boot_memory	1: Boot Flash = 16 bits 0: Boot Flash = 8 bits
0	strap_system_big_endian	1: System is big endian 0: System is little endian
0	strap_pci_client	1: PCI in client (slave) mode 0: PCI in bridge (master) mode
0	strap_pci_memwin1_en	1: PCI memwin 1 enable 0: PCI memwin 1 disable
0	strap_pci_memwin2_en	1: PCI memwin 2 enable 0: PCI memwin 2 disable
0	strap_pci_memwin_size_1	3: 256 MByte window 2: 128 MByte window
0	strap_pci_memwin_size_0	1: 64 MByte window 0: 32 MByte window
1	strap_33_27_MHZ_clock	1: 33 MHz clock output 0: 27 MHz clock output
0	strap_reset_outb_def_value	
0	strap_xtal_adj3	Adjust the 54MHz oscillator bias current
0	strap_xtal_adj2	
0	strap_xtal_adj1	
0	strap_xtal_adj0	
0	strap_ebi_rom_size1	3: NOR: 4 MBytes NAND: Disable ECC 2: NOR: 8 MBytes NAND: Disable ECC
0	strap_ebi_rom_size0	1: NOR: 16 MBytes NAND: Ebable ECC 0: NOR 64 MBytes NAND: Ebable ECC

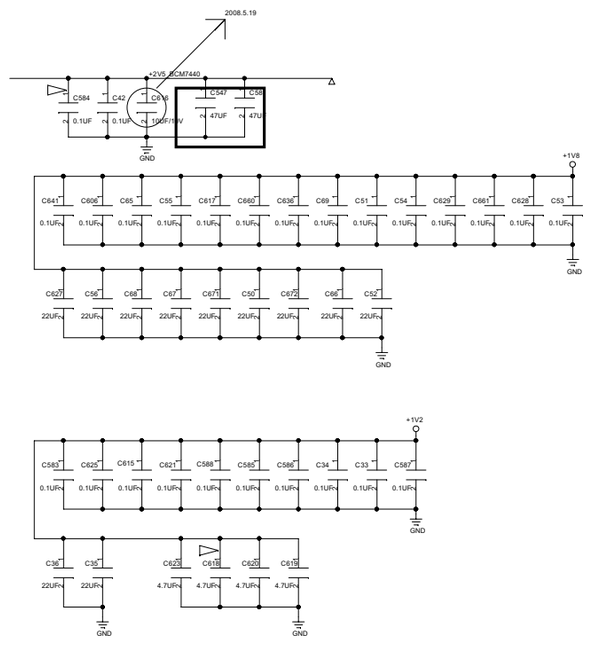


Boot strap option --> Design notes and Layout Guidelines:

1- Note these configuration resistors do not need to be close to the BCM7440. So, place them at the destination of the trace.
It will clear the BCM7440 area and help the chip layout.

BCM7440 Power

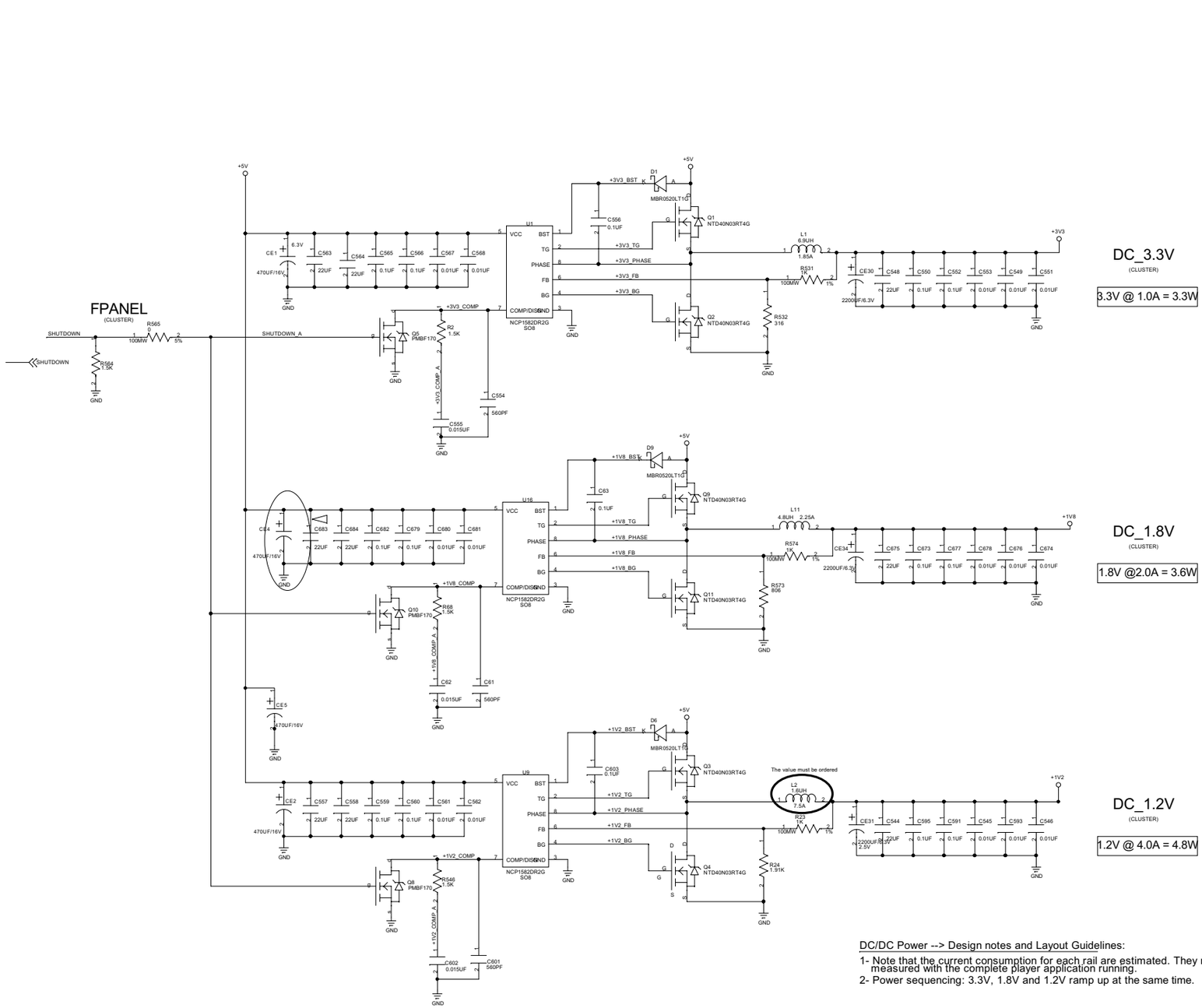




Place 4.7uF directly
under chip.

Main Board Electric Diagram: DC/DC CONVERTERS

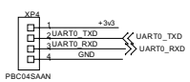
DC/DC Converters

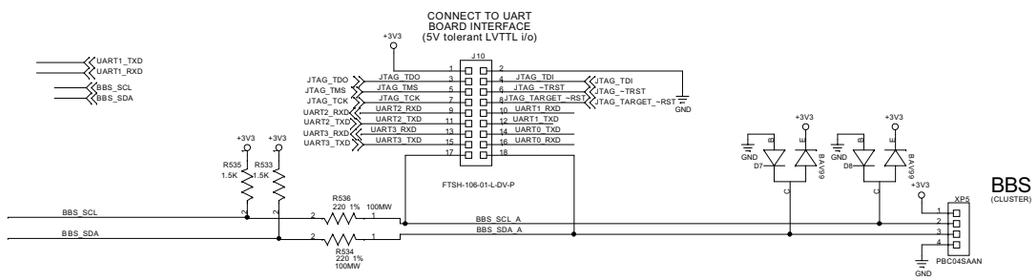


DC/DC Power --> Design notes and Layout Guidelines:

1- Note that the current consumption for each rail are estimated. They must be must be measured with the complete player application running.
2- Power sequencing: 3.3V, 1.8V and 1.2V ramp up at the same time.

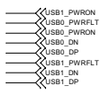
RTC, FPANEL, UART, BBS
RESET, CLOCK, GPIO, IRQ

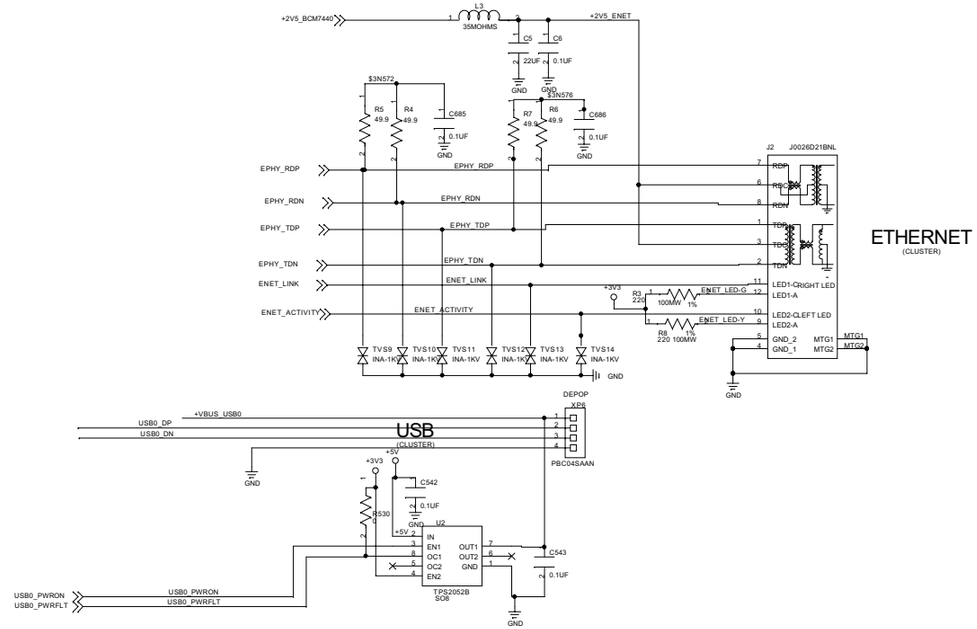




Ethernet, SATA, IDE

Main Board Electric Diagram: Ethemet, SATA, USB

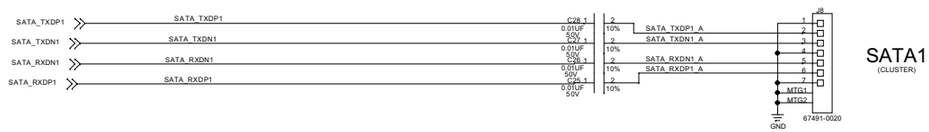




ETHERNET
(CLUSTER)

ETHERNET : Design notes and Layout Guidelines:

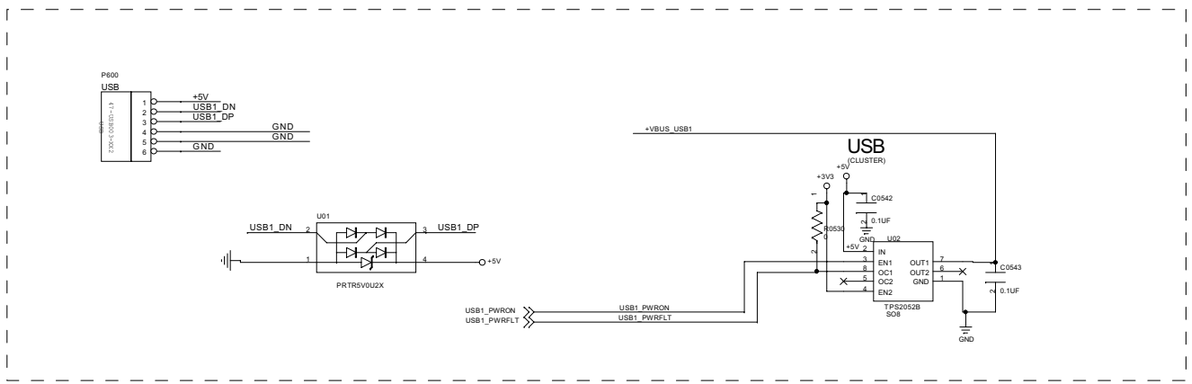
1- Ethernet Data DP/DN traces must be routed as 100 Ohms Differential pairs.
2- Match trace lenght of DP/DN differential pairs. 100 mils max within a pair.
3- Route differential pairs above the GND plane. Do not split the GND plane under differential pairs.
4- Use minimum number of VIA.
5- When possible, use higher clearance distance between differantials pairs and any others traces (>15 mils).
6- For fanout facility, all the ethernet terminations can be place close to the connector.
7- Use a 15 mils trace to route 2.5V.
8- Place EPHY_RDAC resistor close to BCM7440.



SATA1
(CLUSTER)

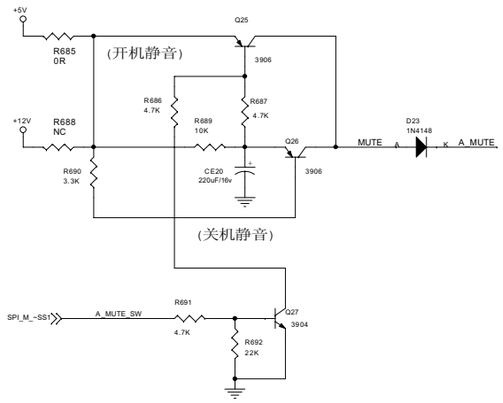
SATA : Design notes and Layout Guidelines:

* SATA speed is 1.5Gbs, keep traces as short as possible.
1- SATA Data DP/DN traces must be routed as 100 Ohms Differential pairs.
2- Match trace lenght of DP/DN differential pairs. 20 mils max within a pair.
3- Route differential pairs above the GND plane. Do not split the GND plane under differential pairs.
4- Use minimum number of VIA.
5- When possible, use higher clearance distance between differantials pairs and any others traces (>15 mils).
6- Place series capacitors close to connectors.
7- Place SATA 25MHz xtal and passive component close close to BCM7440.

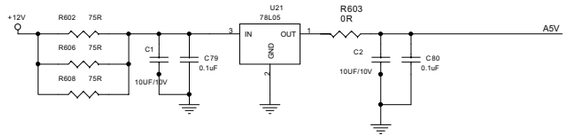


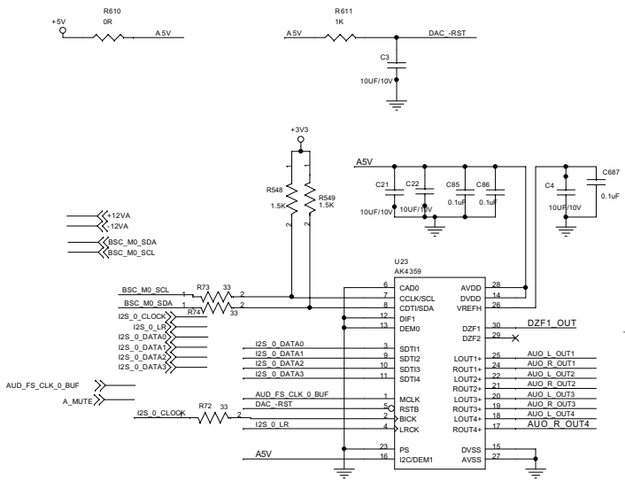
7.1 AUDIO OUTPUTS

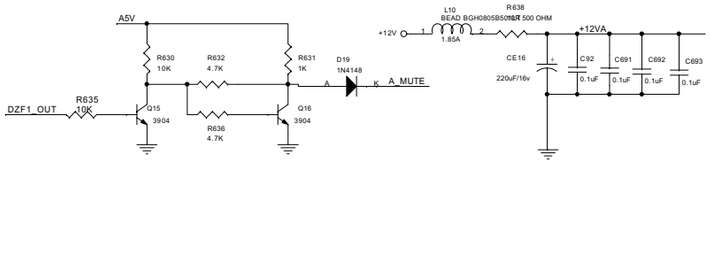
mute circuit

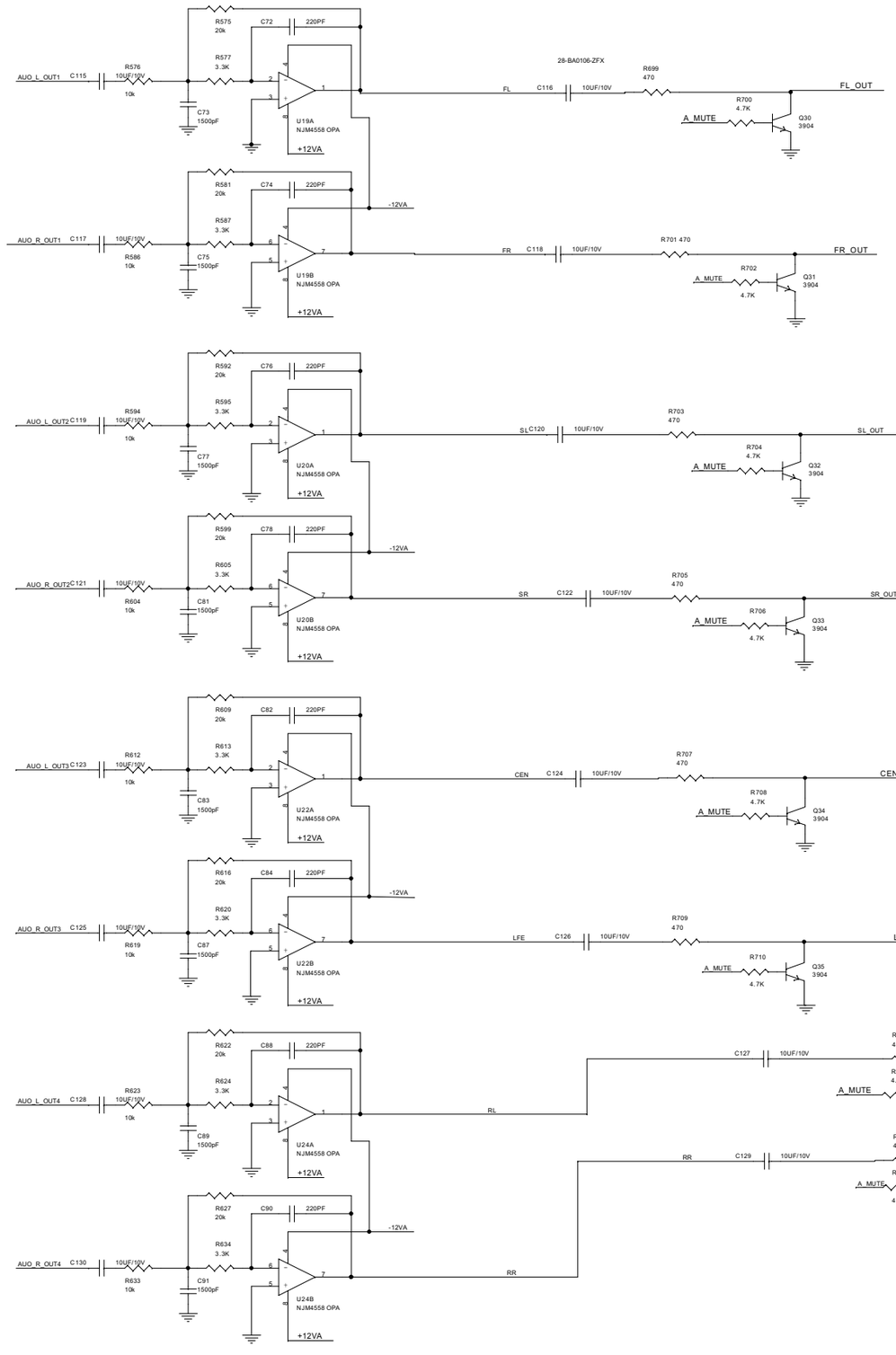


28-CC0106-KBX(10UF/16V 1206)
28-BA0106-ZFX(10UF/16V 0805)









MCU

Main Board Electric Diagram: MCU