DDX-1080/DDX-1060/DDX-1050

All-Digital High Efficiency Power Amplifiers

FEATURES

- HIGH OUTPUT CAPABILITY
- **DDX® Full-Bridge Mode:**
  - **DDX-1080:** 1 x 90 / 80 W, 8Ω / 6Ω, < 10% THD
  - **DDX-1060:** 1 x 80 / 62 W, 8Ω / 6Ω, < 10% THD
  - **DDX-1050:** 1 x 65 / 50 W, 8Ω / 6Ω, < 10% THD
- **Binary Half-Bridge Mode:**
  - **DDX-1080:** 2 x 45 W, 4Ω, < 10% THD
  - **DDX-1060:** 2 x 40 W, 4Ω, < 10% THD
  - **DDX-1050:** 2 x 32 W, 4Ω, < 10% THD
- SINGLE SUPPLY (+9V to +40V)
- COMPACT SURFACE MOUNT PACKAGE
- HIGH EFFICIENCY, > 90% @ 8 ohms
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION

BENEFITS

- COMPLETE SURFACE MOUNT DESIGN
- POWER SUPPLY SAVINGS

APPLICATIONS

- DIGITAL POWERED SPEAKERS
- PC SOUND CARDS
- CAR AUDIO
- SURROUND SOUND SYSTEMS
- DIGITAL AUDIO COMPONENTS

1.0 GENERAL DESCRIPTION

The DDX-1080, DDX-1060 and DDX-1050 power devices are monolithic, single channel H-Bridges that can provide audio power up to:

- 90 watts one channel @10%THD, 8Ω (DDX-1080)
- 80 watts one channel @10%THD, 8Ω (DDX-1060)
- 65 watts one channel @10%THD, 8Ω (DDX-1050)

at very high efficiency.

Each device contains a logic interface, integrated bridge drivers, high efficiency MOSFET output transistors and protection circuitry. Each device may be used in DDX® Mode as a single bridge or, alternatively in Binary Mode, it may be configured as either a single bridge or (at lower power output) a dual half-bridge.

The benefits of the DDX® amplification system are: an all-digital design that eliminates the need for a digital to analog converter (DAC), and the high efficiency operation derived from the use of Apogee's patented damped ternary pulse width modulation (PWM). This approach provides an efficiency advantage over conventional PWM designs of more than three times the efficiency of typical Class A/B amplifiers with music input signals.

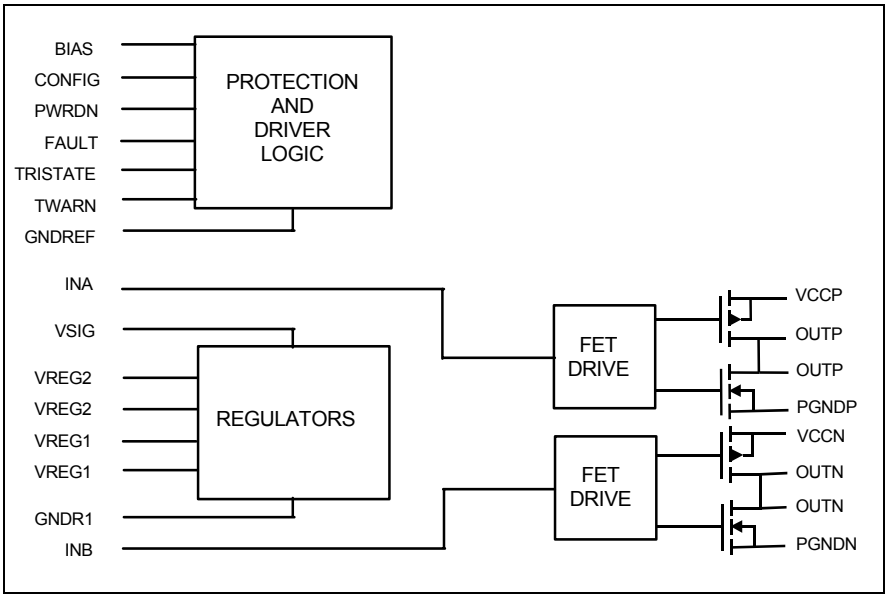


Figure 1 - Block Diagram

1.1 Absolute Maximum Ratings [Note 1]

SYMBOL	PARAMETER	VALUE	UNIT
V_{CC}	Power supply voltage	45	V
V_L	Input logic reference	5.5	V
P_{TOT}	Power Dissipation, $T_{heat\text{-}spreader}$ = 25°C [See Figure 4]	50	W
T_j	Operating junction temperature range	0 to +150	°C
T_{stg}	Storage temperature range	-40 to +150	°C

Note 1 - Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.2 Recommended Operating Conditions [Note 2]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Power supply voltage	9.0		40.0	V
V_L	Input logic reference	2.7	3.3	5.0	V
T_A	Ambient Temperature	0		70	°C

Note 2 - Performance not guaranteed beyond recommended operating conditions.

1.3 Thermal Data

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$\theta_{J\text{-}C}$	Thermal resistance, junction-to-case (heat spreader)			2.5	°C/W
$T_{j\text{-}SD}$	Thermal shut-down junction temperature		150		°C
T_{WARN}	Thermal warning temperature		130		°C
T_{hSD}	Thermal shut-down hysteresis		25		°C

1.4 Electrical Characteristics.

[Refer to circuit in Figure 14] Unless otherwise specified, performance is measured using the DDX-8001/DDX-8229 processor family, V_{CC}=34V, VL=3.3V, fsw=384kHz, T_C=25°C, R_L=8Ω.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNIT
		V_{CC}	THD+N	R_L				
$P_{O\text{-}DF}$ (DDX® Full Bridge Mode) [Figure 14]	DDX-1080 - Power Per Channel [Note 3]	40V	<10%	8Ω		90		W_{RMS}
			<1%			72		
	DDX-1080 - Power Per Channel [Note 4]	32V	<10%	6Ω	80			
			<1%		62			
	DDX-1060 - Power Per Channel [Note 4]	37V	<10%	8Ω	80			
			<1%		62			
	DDX-1060 - Power Per Channel [Note 4]	29V	<10%	6Ω	62			
			<1%		50			
	DDX-1050 - Power Per Channel [Note 4]	33V	<10%	8Ω	65			
			<1%		50			
$P_{O\text{-}Bin}$ (Binary Half-Bridge Mode) [Figure 16]	DDX-1080 - Power Per Channel	40V	<10%	4Ω		45		W_{RMS}
			<1%			35		
	DDX-1060 - Power Per Channel [Note 4]	37V	<10%	4Ω	40			
			<1%		32			
	DDX-1050 - Power Per Channel [Note 4]	32V	<10%	4Ω	32			
			<1%		25			

Note 3 - Maximum Power Limited to < 1 second.
Note 4 – Power Output Limited by Minimum Current Limit.

1.4 Electrical Characteristics (continued) [Refer to circuit in Figure 14] Unless otherwise specified, performance is measured using the DDX-8001/DDX-8229 processor family, V_{CC} =34V, V_L=3.3V, fsw=384kHz, T_C=25°C, R_L=8Ω.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
THD+N	Total Harmonic Distortion + Noise, [Note 5]	Po = 1 Wrms		0.06		%
		Po = 50 Wrms		0.08		
SNR	Signal to Noise Ratio, DDX® Mode	A-Weighted (relative to full scale)		98		dB
	Signal to Noise Ratio, Binary Half-Bridge Mode, [Note 5]			92		
η	Peak Efficiency, DDX® Mode	Po = 1 x 65 W, 8Ω, 10% THD		90		%
	Peak Efficiency, Binary Half-Bridge Mode	Po = 2 x 32 W, 4Ω, 10% THD		88		
I_{SC}	Speaker Output Short-Circuit Protection Limit per Bridge	DDX-1080	4.5	6	8	A
		DDX-1060	4.0	6	8	
		DDX-1050	3.5	6	8	
$R_{ds\text{-}on}$	Power MOSFET output resistance	I_d = 1A		200	270	mΩ
g_N	Power Nchannel $R_{ds\text{-}on}$ matching	I_d = 1A	95			%
g_P	Power Pchannel $R_{ds\text{-}on}$ matching	I_d = 1A	95			%
I_{dss}	Power Pchannel/Nchannel leakage	V_{CC} = 35 V			50	uA
UVL	Under-voltage Lockout Threshold			7	9	V
I_{PD}	V_{CC} supply current, Power-down	PWRDN = 0		1	3	mA
$I_{CC\text{-}tri}$	V_{CC} supply current, Tri-state	TRISTATE = 0		22		mA
I_{CC}	DDX® mode V_{CC} supply current	1-Channel switching at 384kHz.		49		mA
	Binary mode V_{CC} supply current	2-Channel switching at 384kHz.		53		
t_{on}	Turn-on delay time	Resistive load			100	ns
t_{off}	Turn-off delay time	Resistive load			100	ns
t_r	Rise time	Resistive load			25	ns
t_f	Fall Time	Resistive load			25	ns
V_{IL}	Low logic input voltage: PWRDN, TRISTATE pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V	0.7 0.8 0.85			V
	Low logic input voltage: INA, INB pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V	1.05 1.35 2.2			
V_{IH}	High logic input voltage: PWRDN, TRISTATE pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V			1.5 1.7 1.85	V
	High logic input voltage: INA, INB pins	V_L = 2.7V V_L = 3.3V V_L = 5.0V			1.65 1.95 2.8	
I_{fault}	Output Sink Current, FAULT, TWARN pins	Fault Active		1		mA
P_{Wmin}	Minimum output pulse width	No load	70		150	ns

Note 5 – Performance Characteristics obtained using a DDX-8001/DDX-8229 controller.

1.5 Logic Truth Table

TRISTATE	InA	InB	OUTP	OUTN	OUTPUT MODE
0	X	X	OFF	OFF	Hi-Z
1	0	0	GND	GND	DAMPED
1	0	1	GND	VCC	NEGATIVE
1	1	0	VCC	GND	POSITIVE
1	1	1	VCC	VCC	Not Used

2.0 DDX-1080, DDX-1060 and DDX-1050 Pin Function Description:

2.1 PWM Inputs

	Pin No.	Description
INA	31	A logic input signal
INB	32	B logic input signal

2.2 Control/Miscellaneous

Pin Name	Pin No.	Description
PWRDN	25	Power Down (0=Shutdown, 1= Normal).
TRI-STATE	26	Tri-State (0=All MOSFETS Hi-Z, 1=Normal).
FAULT [Note 6]	27	Fault output indicator; Overcurrent, Overvoltage or Overtemperature (0=Fault, 1=Normal).
TWARN [Note 6]	28	Thermal warning output (0=Warning T_J >= 130°C, 1=Normal).

Note 6: FAULT and TWARN outputs are open-drain

2.3 Power Outputs for DDX® Mode or Binary Full Bridge Mode [Note 7] OR Binary Half-Bridge Mode [Note 8]

Pin Name	Pin No.	Description
OUTA	8, 9	A output: DDX/Binary positive reference OR ½ bridge positive reference
OUTB	2, 3	B output: DDX/Binary negative reference OR ½ bridge positive reference

Note 7: DDX® and Binary Full-Bridge outputs are bridged. The output OUTA produces signals in phase with the input. The output OUTB produces signals out of phase with the input.

Note 8: Half-Bridge Binary Mode outputs are NOT bridged. All outputs produce signals in phase with the respective inputs.

2.4 Power Supplies

Pin Name	Pin No.	Description
VCC	4, 12, 15	Power
PGND	5, 6, 13	Power grounds
VREG1	21, 22	Internal 5V regulator voltage (referred to Ground) requires bypass capacitor.
VREG2	33, 34	Internal 5V regulator voltage (referred to VSIG) requires bypass capacitor.
VSIG	35, 36	Signal Positive supply.
VL [Note 11]	23	Logic reference voltage.
GNDREF	19	Logic reference ground.
GNDS	1	Substrate ground.
GNDR1	20	Internal regulator ground.
N.C.	7, 10, 11, 14, 16, 17, 18, 24, 29, 30	No Connection

Note 9: V_L (Logic Reference Voltage) is recommended to be powered and stable prior to Vcc achieving > 7V to assure proper power up sequence. V_L is recommended to remain powered and stable until after Vcc has decayed below 7V during power removal.

3.0 DDX-1080, DDX-1060 and DDX-1050 POWER DEVICES

The DDX-1080, DDX-1060 and DDX-1050 Power Devices are single channel H-Bridges that can deliver more than 90/80/65 watts per channel (<10%THD) of audio output power at very high efficiency. They convert both DDX® and binary-controlled PWM signals into audio power at the load. Each includes a logic interface, integrated bridge drivers, high efficiency MOSFET outputs, and thermal and short circuit protection circuitry. In DDX® mode, two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a bridge configuration, according to Apogee's patented damped ternary PWM. In Binary Mode operation, both Full Bridge and Half Bridge Modes are supported. These devices include over-current and thermal protection as well as under-voltage lockout with automatic recovery. A thermal warning status is also provided.

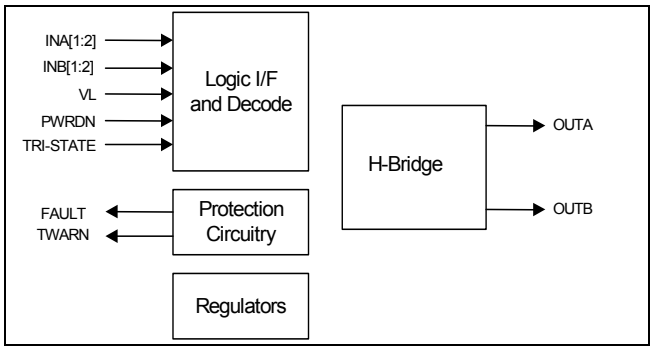


Figure 2 – DDX-1080, DDX-1060 and DDX-1050 Block Diagram, Full- Bridge DDX® or Binary Modes

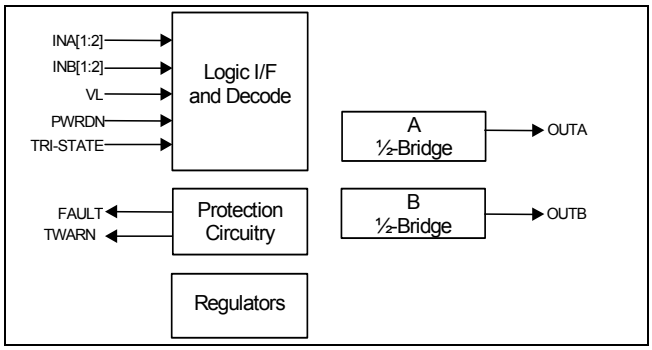


Figure 3 – DDX-1080, DDX-1060 and DDX-1050 Block Diagram, Binary Half-Bridge Mode

3.1 Logic Interface and Decode

The DDX-1080, DDX-1060 and DDX-1050 power outputs are controlled using one or two logic level timing signals. In order to provide a proper logic interface, the V_L input must operate at the same voltage as the DDX® controller logic supply. VL (Logic Reference Voltage) is recommended to be powered and stable prior to Vcc achieving > 7V to assure proper power up sequence. VL is recommended to remain powered and stable until after Vcc has decayed below 7V during power removal.

3.2 Protection Circuitry

The DDX-1080, DDX-1060 and DDX-1050 include protection circuitry for over-current and thermal overload conditions. A thermal warning pin TWARN is activated low (open-drain MOSFET) when the IC temperature exceeds 130°C, in advance of the thermal shutdown protection. When a fault condition is detected (logical OR of over-current and thermal), an internal fault signal acts to immediately disable the output power MOSFETs, placing both H-bridge in a high impedance state. At the same time an open-drain MOSFET connected to the FAULT pin is switched on.

There are two possible modes subsequent to activating a fault. The first is a SHUTDOWN mode. With FAULT (pull-up resistor) and TRI-STATE pins independent, an activated fault will disable the device, signaling low at the FAULT output. The device may subsequently be reset to normal operation by toggling the TRI-STATE pin from High to Low to High using an external logic signal.

The second is an AUTOMATIC recovery mode. This is depicted in the application circuit in Figure 14. The FAULT and TRI-STATE pins are shorted together and connected to a time constant circuit comprising R_T and C_T. An activated FAULT will force a reset on the TRI-STATE pin causing normal

operation to resume following a delay determined by the time constant of the circuit. If the fault condition is still presented, the circuit operation will continue repeating until such time as the fault condition is removed. An increase in the time constant of the circuit will produce a longer recovery interval. Care must be taken in the overall system design so as not to exceed the protection thresholds under normal operation.

3.3 Power Outputs

The DDX-1080, DDX-1060 and DDX-1050 power and output pins are duplicated to provide a low impedance path for the device's bridged outputs. All duplicate power, ground and output pins must be connected for proper operation. The PWRDN or TRI-STATE pins should be used to set all MOSFETS to the Hi-Z state during power-up until the logic power supply, V_L, is settled.

3.4 ADDITIONAL INFORMATION

3.5 Output Filter

A passive two-pole low-pass filter is used on the DDX-1080, DDX-1060 and DDX-1050 power outputs to reconstruct an analog signal. System performance can be significantly affected by the output filter design and choice of components. (See appnote: AN-15, Component Selection for DDX Amplifiers.) A filter design for 6Ω/8Ω loads is shown in the Typical Application Circuit in Figure 14. Figure 16 shows a filter for ½ bridge mode, 4Ω loads.

3.6 Power Dissipation & Heat Sink Requirements

The power dissipated within the device will depend primarily on the supply voltage, load impedance, and output modulation level.

The surface mount package of the DDX-1080, DDX-1060 and DDX-1050 include an exposed thermal slug on the top of the device to provide a direct thermal path from the integrated circuit to the heatsink. Careful consideration must be given to the overall thermal design. See Figure 4 for power derating.

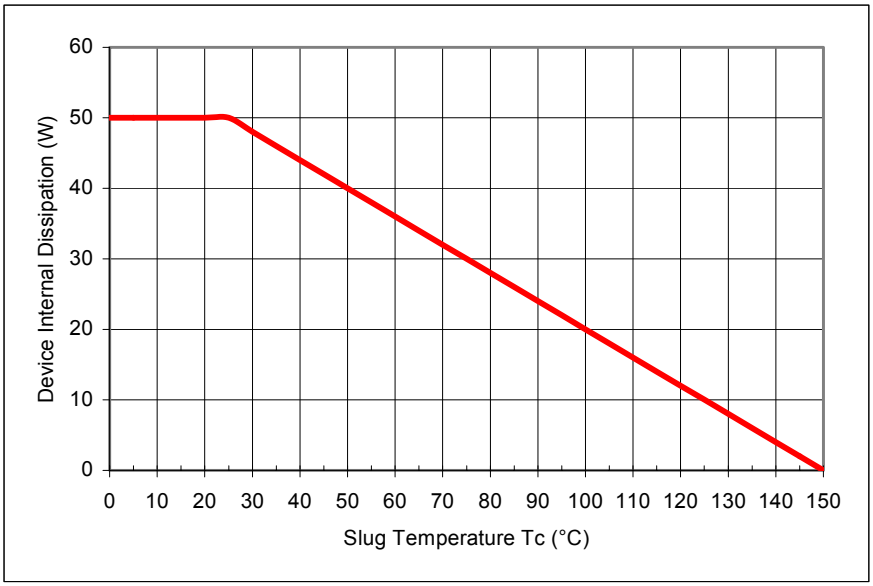


Figure 4 – Power Derating Curve (Typical)

For additional thermal design considerations, see: AN19, Power Device Thermal Calculator.

For additional design considerations with binary mode operation, see application note: AN-16, Applying the DDX-8000/DDX-8228 in Binary Mode.

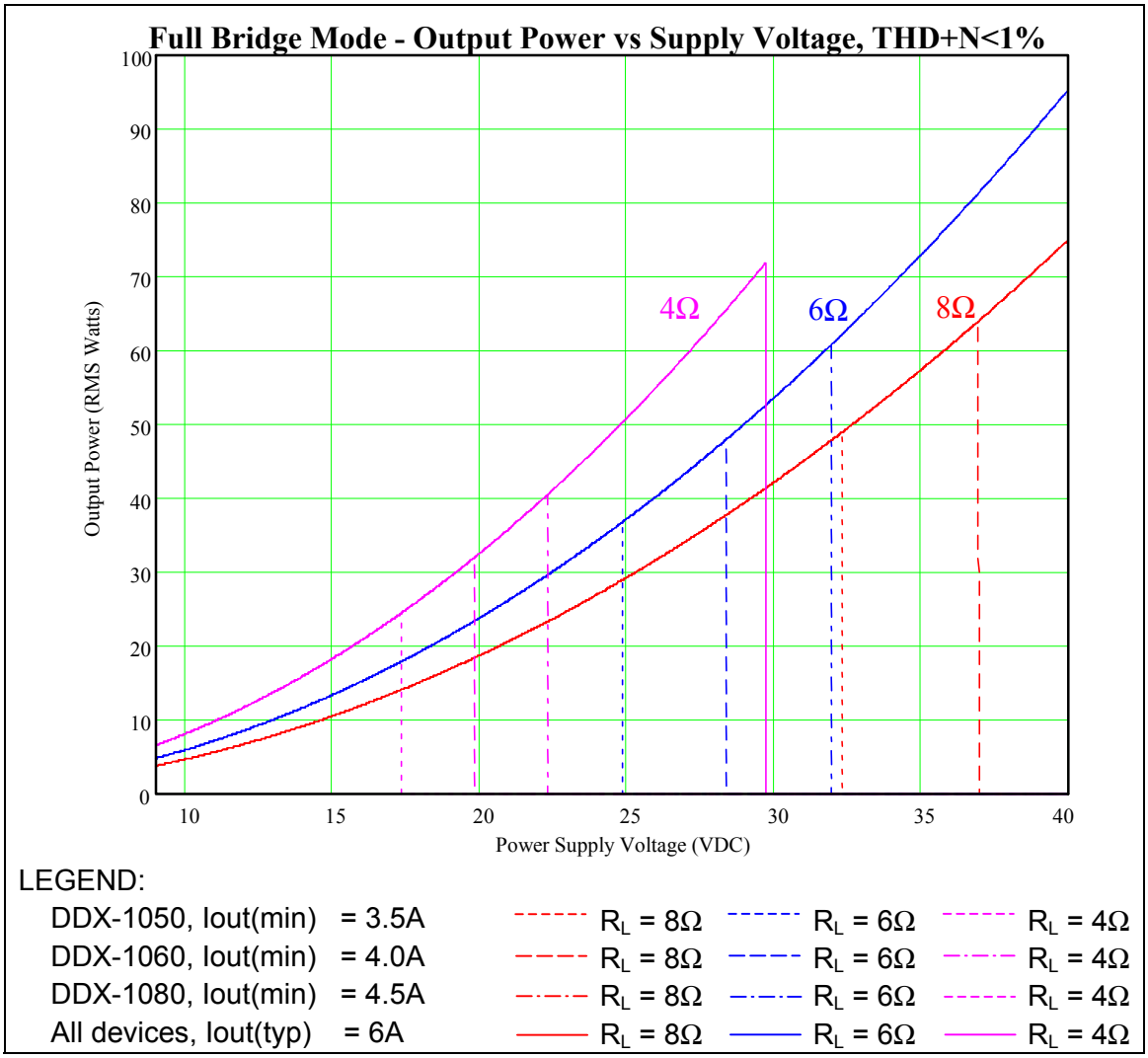


Figure 5 - Full Bridge Output Power vs. Supply Voltage, <1% THD.

Figure 5 shows the full-scale output power (0 dB FS digital input with unity amplifier gain) as a function of Power Supply Voltage for 4, 6, and 8 Ohm loads in either DDX® Mode or Binary Full Bridge Mode. Output power is constrained for higher impedance loads by the maximum voltage limit of the DDX-1080, DDX-1060 and DDX-1050 ICs and by the over-current protection limit for lower impedance loads. The minimum threshold for the over-current protection circuit is 4.5/4.0/3.5A (at 25 ºC) but the typical threshold is 6A. Solid curves depict typical output power capability of each device. Dotted and dashed curves depict the output power capability constrained to the minimum current specification of the DDX-1050, DDX-1060 and DDX-1080 respectively. The output power curves assume proper thermal management of the power device's internal dissipation. See Figure 4.

NOTE: Output power at 10% THD is approximately 30% higher.

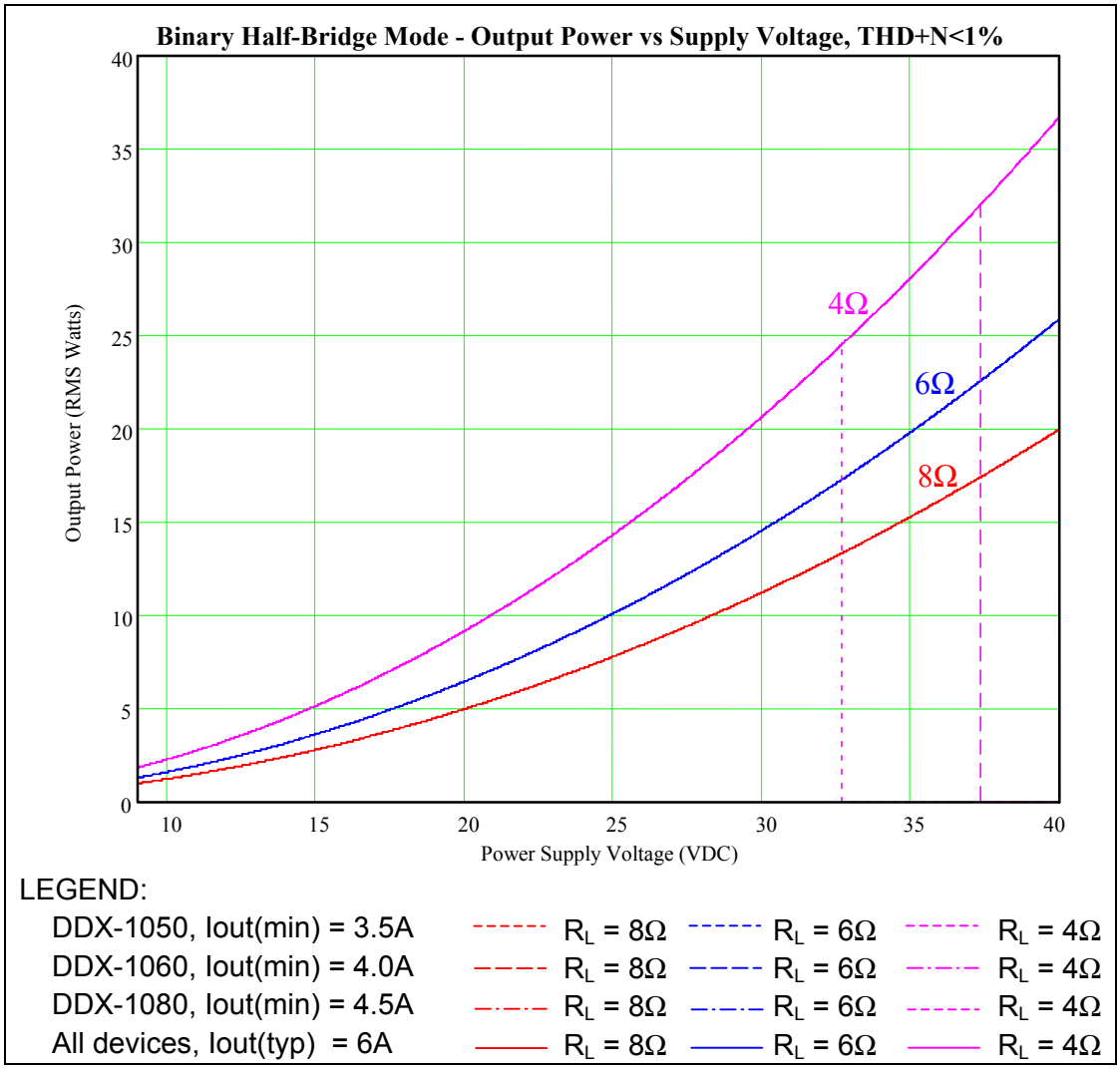


Figure 6 - Half-Bridge Binary Mode Output Power vs Supply, <1% THD
(NOTE: Curves taken at f = 1 kHz and using a 330uF blocking capacitor.)

Figure 6 depicts the output power as a function of power supply voltages for loads of 4, 6, and 8 Ohms when the DDX-1080, DDX-1060 and DDX-1050 are operated in a half-bridge Binary Mode. Solid curves depict typical performance and dotted and dashed curves depict the minimum current limit for the DDX-1050, DDX-1060 and DDX-1080 respectively. Once again, the output power curves assume proper thermal management of the power device's internal dissipation.

NOTE: Output power at 10% THD is approximately 30% higher.

3.7 Typical Bridge Mode Performance Characteristics.

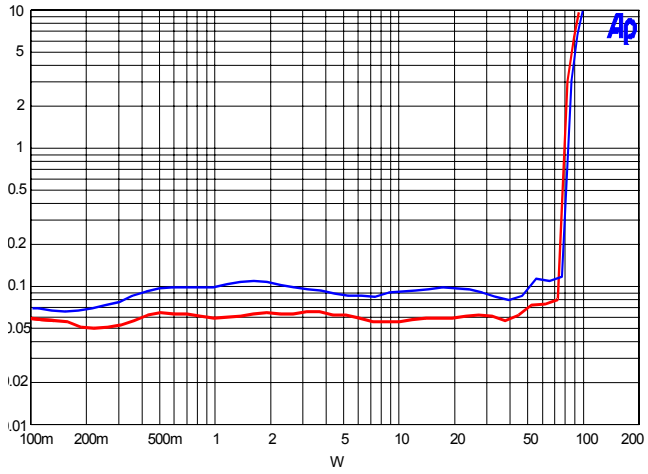


Figure 7 - THD+N vs. Output Power @ 1kHz, using a DDX-8001 controller

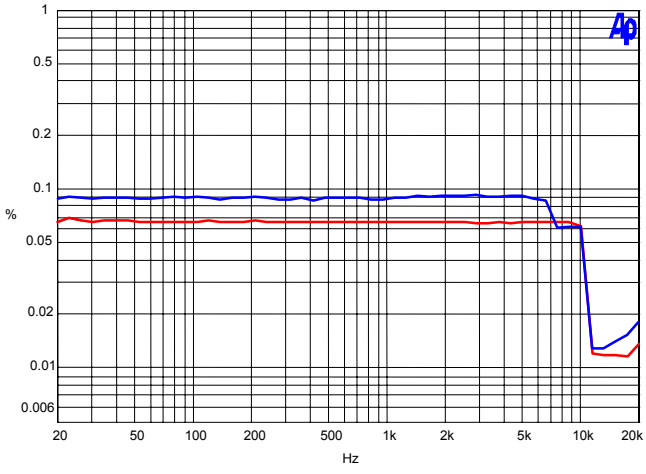


Figure 8 - THD+N vs. Frequency @ 1W, using a DDX-8001 controller

3.8 Typical Binary Half-Bridge Mode Performance Characteristics, V_{CC} = 36 VDC, R_L - 4Ω.

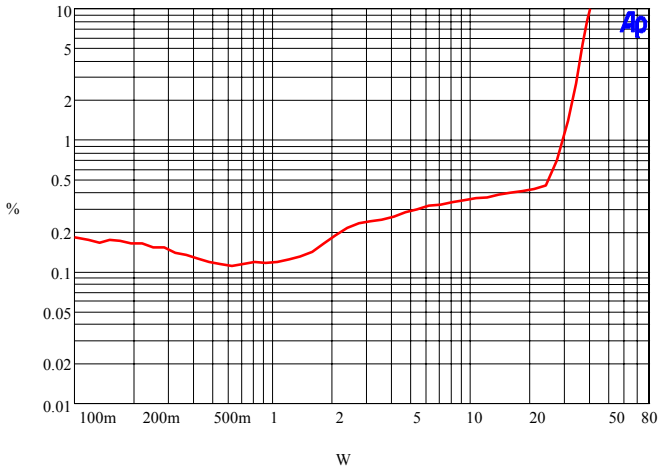


Figure 9 - THD+N vs. Output Power @ 1kHz

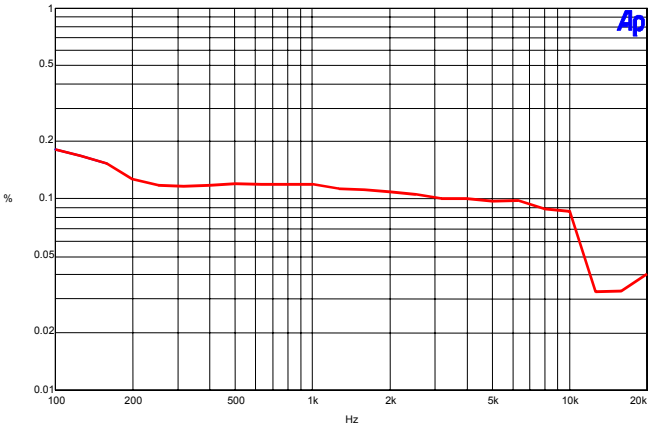


Figure 10 - THD+N vs. Frequency

3.9 Typical DDX-Mode Performance Characteristics at V_{CC} = 36V, 8Ω Load, <1% THD+N.

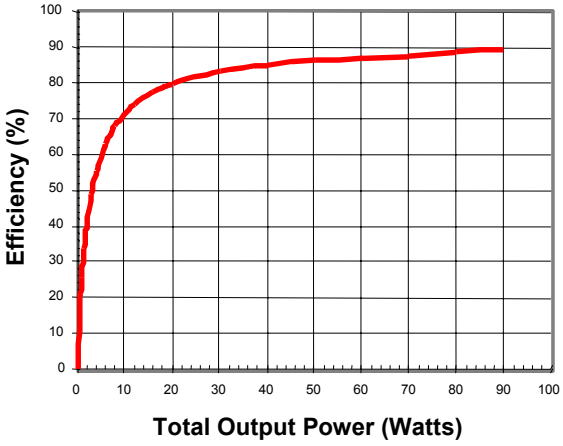


Figure 11 - Typical Efficiency vs. Power Output

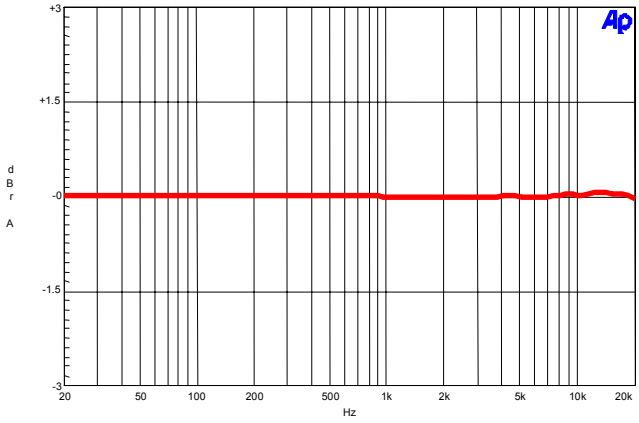


Figure 12 - Typical Frequency Response

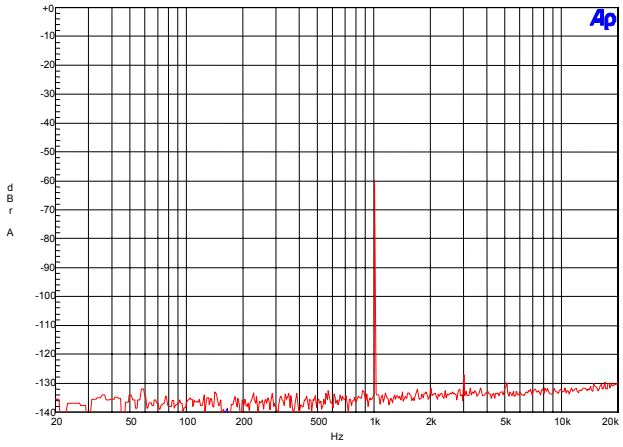


Figure 13 - Typical FFT @ -60 dB,
using a DDX-8001 controller

4.0 APPLICATION REFERENCE DESIGNS.

Apogee can provide reference designs for most applications.
Contact Apogee Technical Support for more information.

4.1 BRIDGE MODE

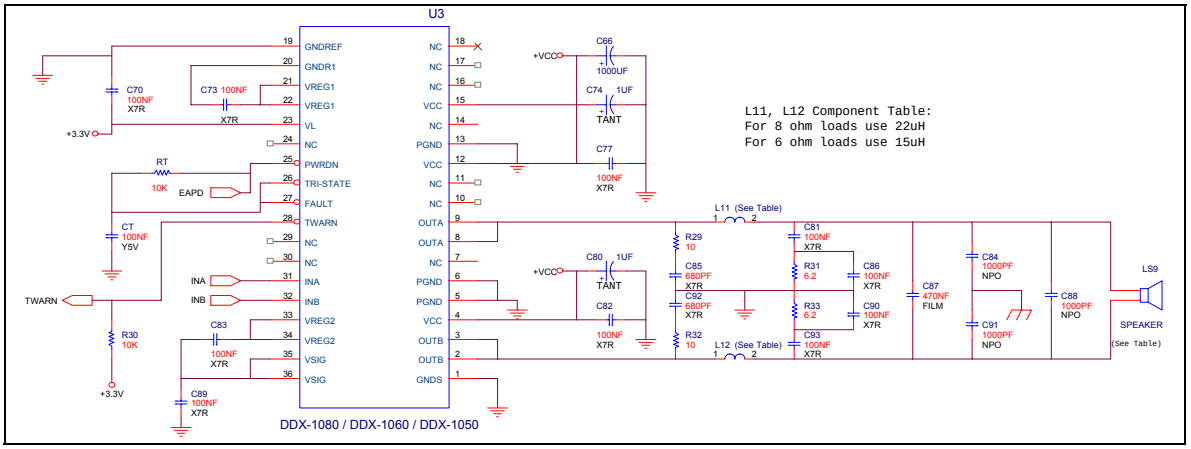


Figure 14 - DDX® Bridge Mode Audio Application Circuit

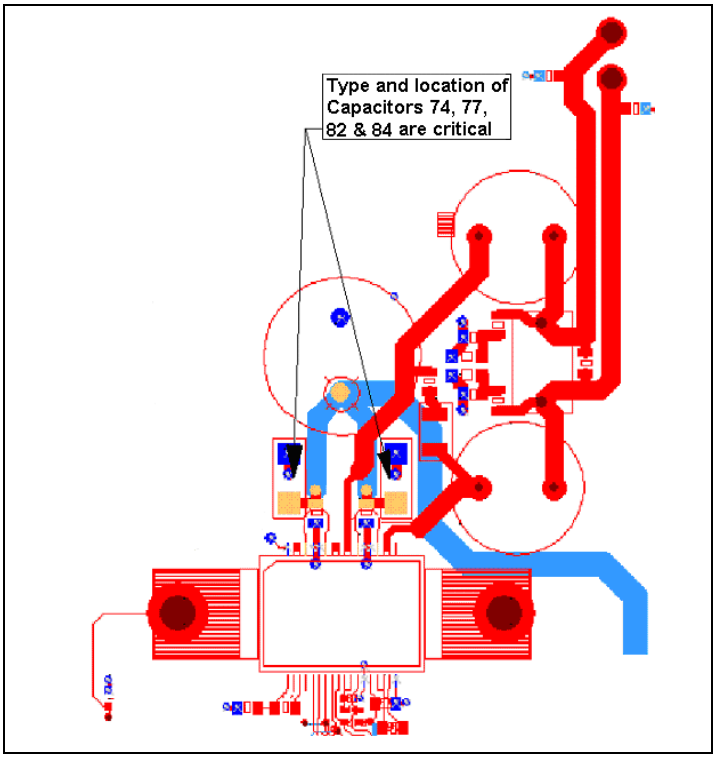


Figure 15 -. Sample DDX® bridge Mode Layout

4.2 BINARY ½ BRIDGE MODE, 2 CHANNEL.

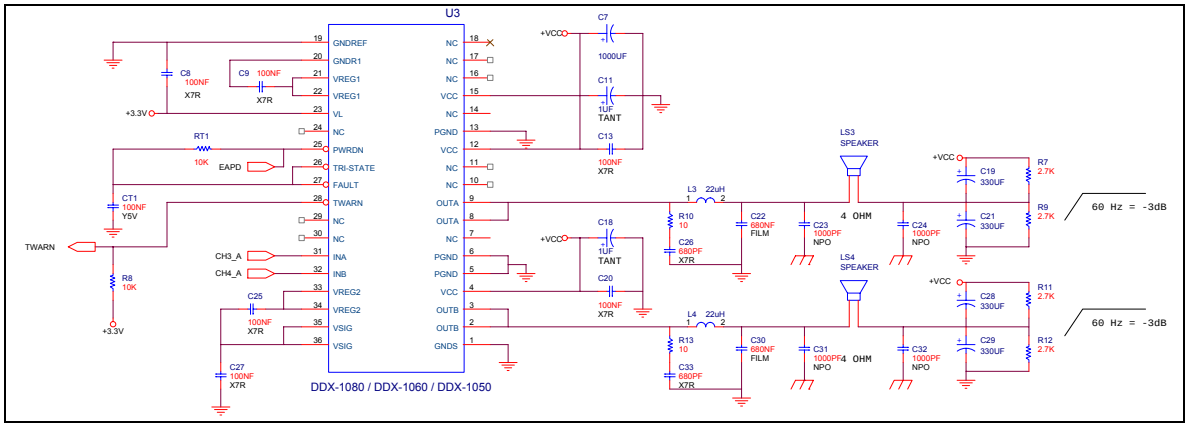


Figure 16 - Binary ½ Bridge Mode, 2-Channel Audio Application Circuit

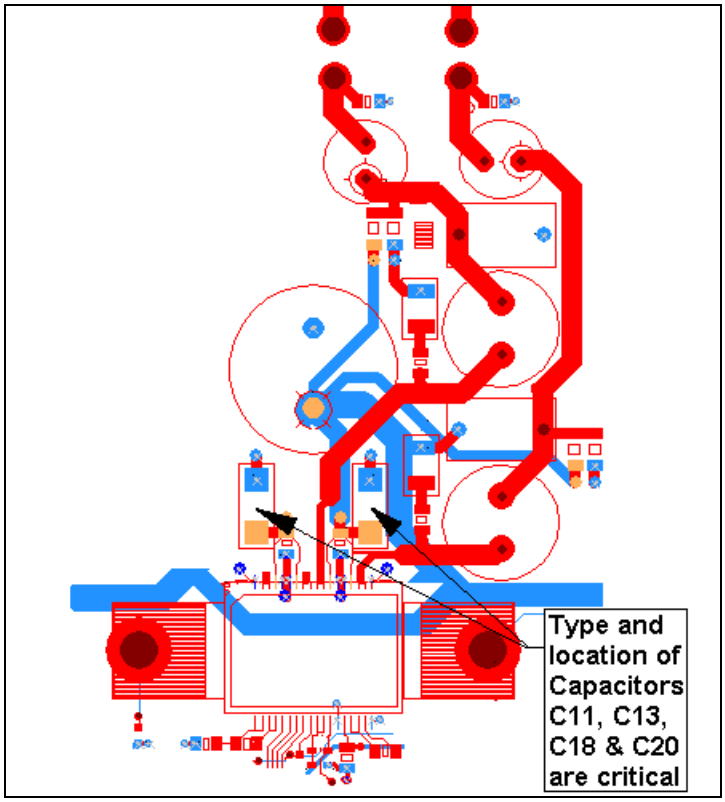
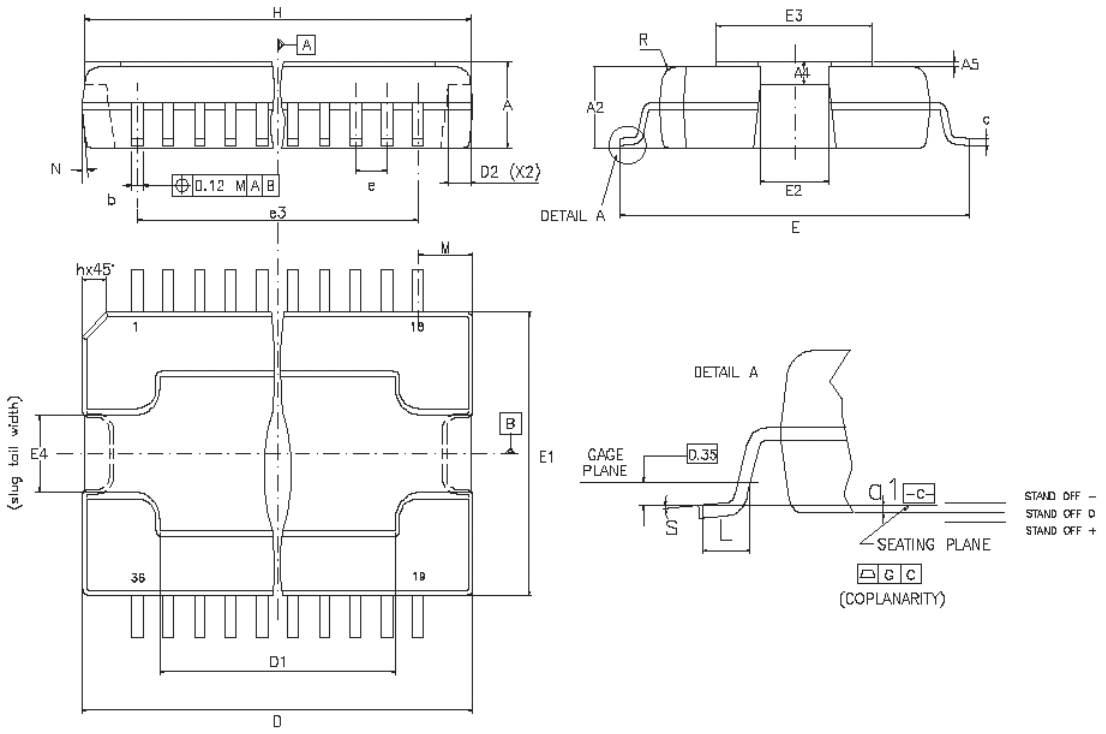


Figure 17 – Sample Binary Mode, 2 Channel Layout

PHYSICAL DIMENSIONS (Dimensions shown in mm)



Reference Dimension	DATA BOOK mm			DATA BOOK inc		
	TYP	MIN	MAX	TYP	MIN	MAX
A	-	3.25	3.5		0.128	0.138
A2	-	-	3.3			0.130
A4	-	0.8	1		0.032	0.039
A5	0.2	-	-	0.008		
a1	-	0.030	-0.040		0.001	-0.002
b		0.22	0.38	0.000	0.009	0.015
c	-	0.23	0.32		0.009	0.013
D	-	15.80	16.00		0.623	0.631
D1	-	9.40	9.80		0.371	0.386
D2	1	-	-	0.039		
E	-	13.9	14.5		0.548	0.572
E1	-	10.9	11.1		0.430	0.438
E2	-	-	2.9			0.114
E3	-	5.8	6.2		0.229	0.244
E4	-	2.9	3.2		0.114	0.126
e	0.65	-	-	0.026		
e3	11.05	-	-	0.436		
G	-	0	0.075		0.000	0.003
H	-	15.5	15.9		0.611	0.627
h	-	-	1.1			0.043
L	-	0.8	1.1		0.032	0.043
M	-	-	-			
N	-	-	10deg			
R	-	-	-			
s	-	-	8deg			

1: "D" and "E1" do not include mold flash or protrusions
Mold flash or protrusions shall not exceed 0.15 mm (0.006") per side
2: No intrusion allowed inwards the leads