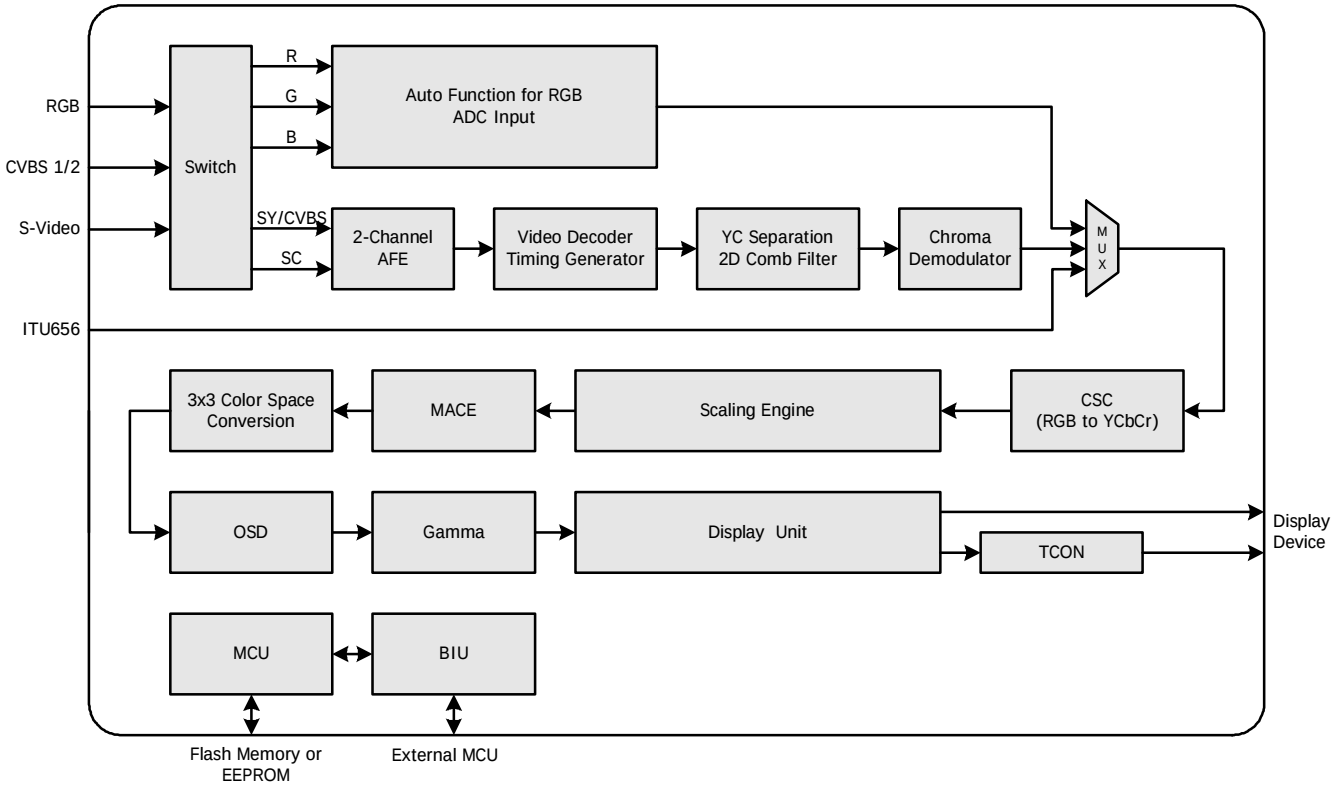
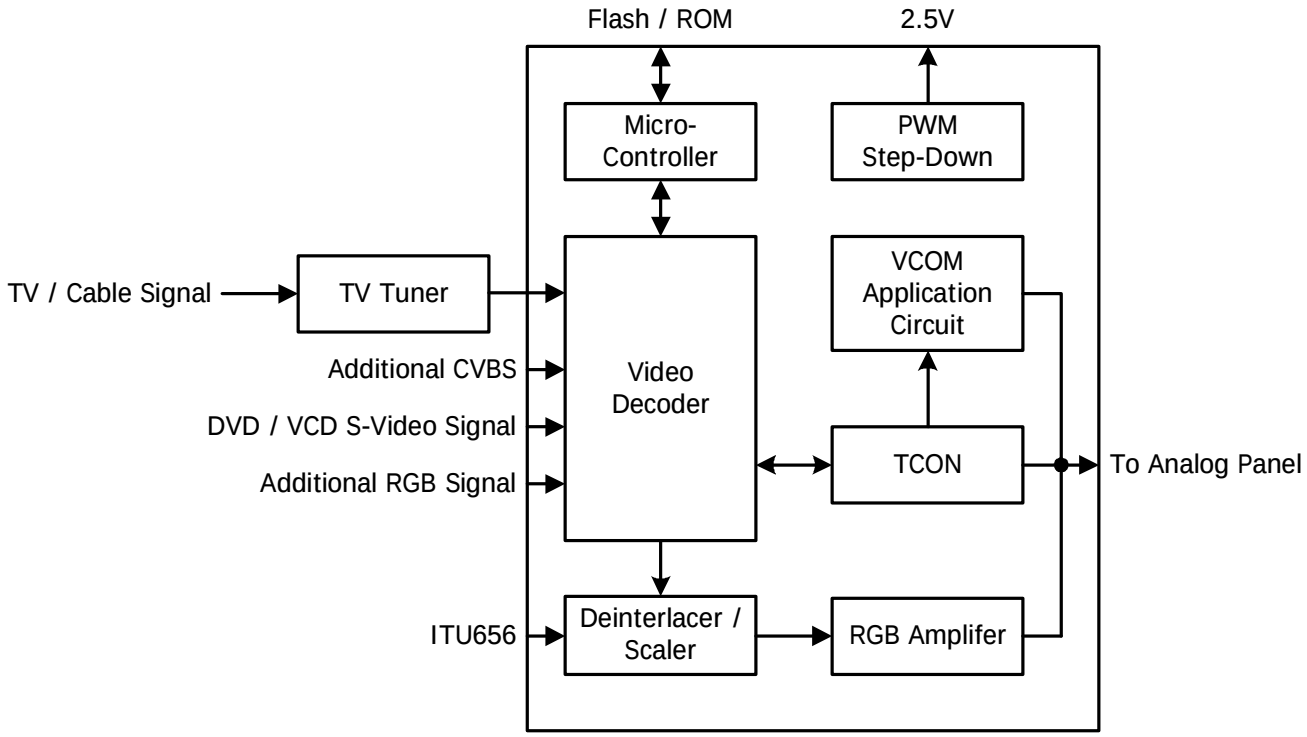
FEATURES

- Video Decoder
  - Supports NTSC, PAL and SECAM video input formats
  - 2D NTSC and PAL comb-filter for Y/C separation of CVBS input
  - Single S-video and/or multiple CVBS inputs
  - Supports closed-caption and V-chip
  - ACC, AGC, and DCGC (Digital Chroma Gain Control)
- Analog Input
  - Supports RGB input format from PC, camcorders and GPS
  - Supports video input 480i, 480p, 576i, 576p, 720p, 1080i; RGB input resolution in 640x480, 800x480, and 800x600 (SVGA)
  - 3-channel low-power 10-bit ADCs integration for RGB
  - Supports RGB composite sync input (CSYNC), SOY, SOG, HSYNC, and VSYNC
  - On-chip clock synthesizer and PLL
  - Auto-position adjustment, auto-phase adjustment, auto-gain adjustment, and auto-mode detection
- Digital Input
  - Supports ITU656 input, progressive ITU656 compatible input format
- Color Engine
  - Brightness, contrast, saturation, and hue adjustment
  - 9-tap programmable multi-purpose FIR (Finite Impulse Response) filter
  - Differential 3-band peaking engine
  - Luminance Transient Improvement (LTI)
  - Chrominance Transient Improvement (CTI)
  - Black Level Extension (BLE)
  - White Level Extension (WLE)
  - Favor Color Compensation (FCC)
  - 3-channel gamma curve adjustment
- Scaling Engine/TCON
  - Supports analog panels with the resolution of 960x234, 1200x234, 1400x234, and more
  - Supports various displaying modes
  - Supports horizontal panorama scaling
- Miscellaneous
  - Built-in MCU
  - 3-wire serial bus interface for configuration setup
  - Built-in VCOM DC level adjusting circuits
  - Built-in internal OSD with 256 programmable fonts, 16-color palettes, and 12-bit color resolution
  - 3-channel low-power 8-bit DAC integration for RGB output, dynamic range 0.1-4.9V
  - Built-in step-down PWM circuits for input 2.5V
  - Built-in VCOM DC/AC level adjustment circuit
  - Supports external OSD
  - Spread spectrum clocks
  - Optional 3.3V / 5V output pads with programmable driving current
  - 128-pin PQFP package

BLOCK DIAGRAM



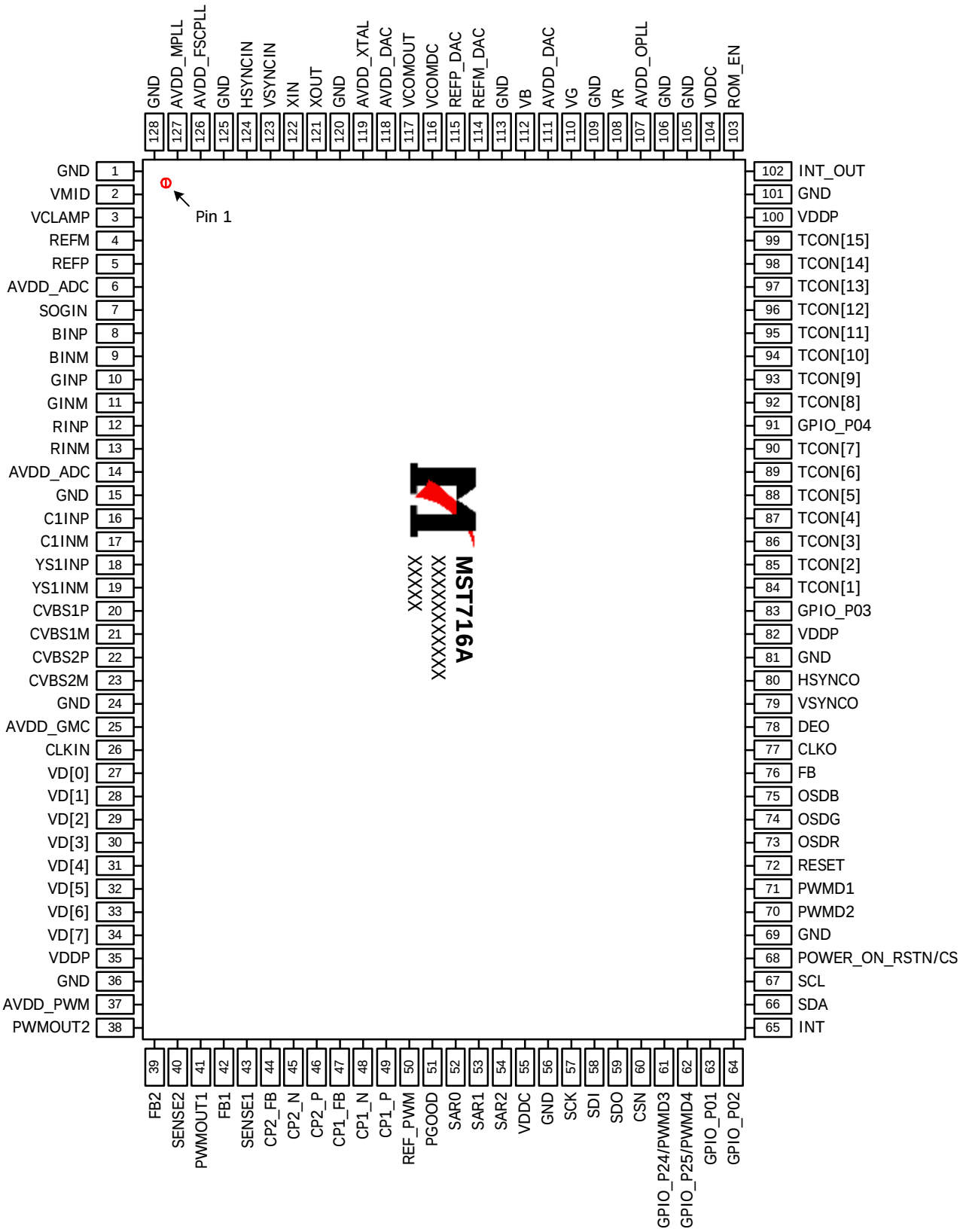
SYSTEM APPLICATION DIAGRAM



GENERAL DESCRIPTION

The MST716A is a high quality ASIC for NTSC/PAL/SECAM car TV application. It receives analog NTSC/PAL/SECAM CVBS and S-Video inputs from TV tuners, DVD or VCR sources, including weak and distorted signals, as well as analog RGB input from GPS systems. Automatic gain control (AGC) and 8-bit 3-channel A/D converters provide high resolution video quantization. With automatic video source and mode detection, users can easily switch and adjust variety of signal sources. Multiple internal adaptive PLLs precisely extract pixel clock from video source and perform sharp color demodulation. Built-in line-buffer supports adaptive 2-D comb-filter, 2-D sharpening, and synchronization stabler in a condense manner. The output format of MST716A supports 3.5”~7” analog TFT-LCD modules.

PIN DIAGRAM (MST716A)



PIN DESCRIPTION

Analog Interface

Pin Name	Pin Type	Function	Pin
VMID		Mid-Scale Voltage Bypass	2
VCLAMP		CVBS/YC Mode Clamp Voltage Bypass	3
REFM		Internal ADC Bottom De-coupling Pin	4
REFP		Internal ADC Top De-coupling Pin	5
SOGIN	Analog Input	Sync-on-Green slicer input	7
BINP	Analog Input	Analog B Input of VGA	8
BINM	Analog Input	Reference Ground for Analog B Input of VGA	9
GINP	Analog Input	Analog G Input of VGA	10
GINM	Analog Input	Reference Ground for Analog G Input of VGA	11
RINP	Analog Input	Analog R Input of VGA	12
RINM	Analog Input	Reference Ground for Analog R Input of VGA	13
C1INP	Analog Input	Analog Chroma Input for TV S-Video1 / Analog Composite Input of TV CVBS4	16
C1INM	Analog Input	Reference Ground for Analog Chroma Input of TV S-Video1 / Analog Composite Input of TV CVBS4	17
YS1INP	Analog Input	Analog Luma Input of TV S-Video1 / Analog Composite Input of TV CVBS3	18
YS1INM	Analog Input	Reference Ground for Analog Luma Input of TV S-Video1 / Analog Composite Input of TV CVBS3	19
CVBS1P	Analog Input	Analog Composite Input for TV CVBS1	20
CVBS1M	Analog Input	Reference Ground for Analog Composite Input of TV CVBS1	21
CVBS2P	Analog Input	Analog Composite Input for TV CVBS2	22
CVBS2M	Analog Input	Reference Ground for Analog Composite Input of TV CVBS2	23
HSYNCIN	Schmitt Trigger Input w/ 5V-tolerant	HSYNC / Composite Sync for VGA Input	124
VSYNCIN	Schmitt Trigger Input w/ 5V-tolerant	VSYNC for VGA Input	123

Digital Video Input Interface

Pin Name	Pin Type	Function	Pin
CLKIN	Input w/5V-tolerant	Sample Clock ITU656 Video Input	26
VD[7:0]	Input w/5V-tolerant	ITU656 Video Data bus	34-27

Analog Panel Output Interface

Pin Name	Pin Type	Function	Pin
VR	Analog Output	Red Channel Output 4.0 Vp-p	108
VG	Analog Output	Green Channel Output 4.0 Vp-p	110
VB	Analog Output	Blue Channel Output 4.0 Vp-p	112
REFM_DAC		DAC Bottom Reference Voltage Decoupling Cap. 1uF to Ground	114
REFP_DAC		DAC Top Reference Voltage Decoupling Cap. 1uF to Ground	115
CLKO	Output	Display Clock Output	77
DEO	Output	Display Enable Output	78
VSYNCO	Output	Vertical Sync Output	79
HSYNCO	Output	Horizontal Sync Output	80
TCON[15:1]	Output	TCON Output	99-92, 90-84

External OSD Interface

Pin Name	Pin Type	Function	Pin
OSDR	Input w/ 5V-tolerant	External OSD R-channel Input	73
OSDG	Input w/ 5V-tolerant	External OSD R-channel Input	74
OSDB	Input w/ 5V-tolerant	External OSD R-channel Input	75
FB	Input w/ 5V-tolerant	External Fast-Blank Input	76

VCOM Interface

Pin Name	Pin Type	Function	Pin
VCOMDC	Analog Output	Reference DC Voltage Output for Common Amplifier	116
VCOMOUT	Analog Output	Pulse Output for Common Voltage.	117

Switching Power and PWM Interface

Pin Name	Pin Type	Function	Pin
PWMOUT2	Output	Switching Pulse Output for DC-DC Converter	38
FB2	Analog Input	Error Voltage Feedback Input Pin for PWM2; voltage = 1.2V	39
SENSE2	Analog Input	Sense Circuit Connection for PWM2	40
PWMOUT1	Output	Switching Pulse Output for DC-DC Converter	41
FB1	Analog Input	Error Voltage Feedback Input Pin for PWM1; voltage = 1.2V	42

Pin Name	Pin Type	Function	Pin
SENSE1	Analog Input	Sense Circuit Connection for PWM1	43
CP2_FB	Analog Input	Error Voltage Feedback Input Pin for CP2; voltage = 1.2V	44
CP2_N	Output	Charge Pump Negative Pulse for DC-DC Negative Voltage Converter	45
CP2_P	Output	Charge Pump Positive Pulse for DC-DC Negative Voltage Converter	46
CP1_FB	Analog Input	Error Voltage Feedback Input Pin for CP1; voltage = 1.2V	47
CP1_N	Output	Charge Pump Negative Pulse for DC-DC Positive Voltage Converter	48
CP1_P	Output	Charge Pump Positive Pulse for DC-DC Positive Voltage Converter	49
REF_PWM		PWM Reference; voltage = 2.4V	50
PGOOD	Output	Power Good Detector	51

Internal MCU Interface with Serial Flash Memory

Pin Name	Pin Type	Function	Pin
SAR2	Analog Input	SAR Low Speed ADC Input 2	54
SAR1	Analog Input	SAR Low Speed ADC Input 1	53
SAR0	Analog Input	SAR Low Speed ADC Input 0	52
SCK	Output	SPI Interface Sampling Clock	57
SDI	Output	SPI Interface Data-In	58
SDO	Input w/ 5V-tolerant	SPI Interface Data-Out	59
CSN	Output	SPI Interface Chip Select	60
GPIO_P01	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	63
GPIO_P02	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	64
INT	Input	Interrupt Input for IR Receiver	65
SDA	I/O w/ 5V-tolerant	3-Wire Serial Bus Data	66
SCL	Input w/ 5V-tolerant	3-Wire Serial Bus Clock	67
POWER_ON_RSTN/CS	Input w/ 5V-tolerant	Power On Reset Signal / Chip Selection for 3-wire Serial	68
GPIO_P03	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	83
GPIO_P04	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	91

Misc. Interface

Pin Name	Pin Type	Function	Pin
RESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware Reset; active high	72
XIN	Analog Input	Crystal Oscillator Input	122
XOUT	Analog Output	Crystal Oscillator Output	121
GPIO_P24/PWMD3	Output	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output; 4mA driving strength	61
GPIO_P25/PWMD4	Output	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output; 4mA driving strength	62
PWMD2	Output	Pulse Width Modulation Output; 4mA driving strength	70
PWMD1	Output	Pulse Width Modulation Output; 4mA driving strength	71
INT_OUT	Output	Mode Detection Interrupt Output	102
ROM_EN	Input	Internal ROM Enable. 0: Disable. 1: Enable.	103

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_ADC	2.5V Power	ADC Power	6, 14
AVDD_GMC	5V Power	GMC Power	25
AVDD_PWM	5V Power	PWM Power	37
AVDD_OPLL	2.5V Power	OPLL Power	107
AVDD_DAC	5V Power	Voltage DAC Power	111, 118
AVDD_XTAL	5V Power	XTAL Power	119
AVDD_FSCPLL	2.5V Power	FSCPLL Power	126
AVDD_MPLL	2.5V Power	MPLL Power	127
VDDC	2.5V Power	Digital Core Power	55, 104
VDDP	3.3V/5V Power	Digital Input/Output Power	35, 82, 100
GND	Ground	Ground	1, 15, 24, 36, 56, 69, 81, 101, 105, 106, 109, 113, 120, 125, 128

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
5.0V Supply Voltages	V_{VDD_50}	-0.3		5.5	V
3.3V Supply Voltages	V_{VDD_33}	-0.3		3.6	V
2.5V Supply Voltages	V_{VDD_25}	-0.3		2.75	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$	-0.3		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}	-0.3		V_{VDD_33}	V
Ambient Operating Temperature (commercial use)	T_A	0		70	°C
Ambient Operating Temperature (extended temp. range)	T_A	-20		80	°C
Storage Temperature	T_{STG}	-40		125	°C
Junction Temperature	T_J			125	°C
Thermal Resistance (Junction to Air) Natural Conversion	θ_{JA}		TBD		°C/W
Thermal Resistance (Junction to Case) Natural Conversion	θ_{JC}		TBD		°C/W

Note: Stress above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

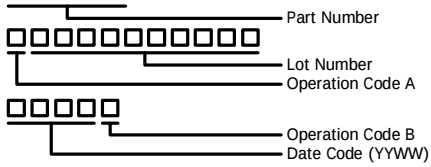
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MST716A	0°C to +70°C	PQFP	128
MST716A-A	-20°C to +80°C	PQFP	128
MST716A-LF	0°C to +70°C	PQFP	128
MST716A-A-LF	-20°C to +80°C	PQFP	128

Note: Product suffix "-LF" represents lead-free version and "-A" represents extended temperature range.

MARKING INFORMATION

MST716A/MST716A-A



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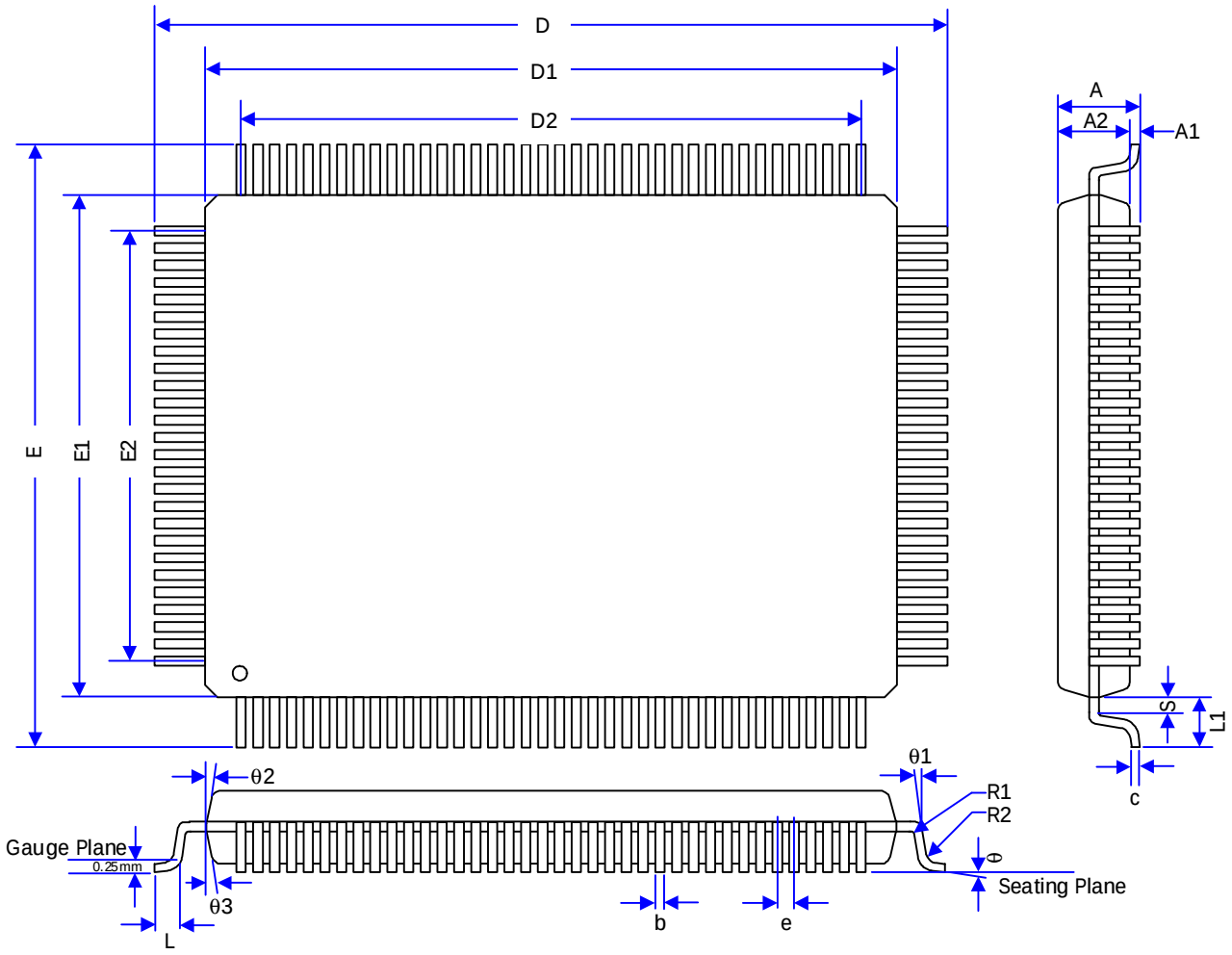
Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST716A comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MST716A_ds_v01	Ÿ Initial release	Nov 2005

MECHANICAL DIMENSIONS



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	3.40	-	-	0.134
A1	0.25	-	-	0.010	-	-
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20			0.913		
D1	20.00			0.787		
D2	18.50			0.728		
E	17.20			0.677		
E1	14.00			0.551		
E2	12.50			0.492		
R1	0.13	-	-	0.005	-	-
R2	0.13	-	0.30	0.005	-	0.012

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
θ	0°	-	7°	0°	-	7°
θ1	0°	-	-	0°	-	-
θ2, θ3 (Alloy)	7° Ref			7° Ref		
θ2, θ3 (Copper)	15° Ref			15° Ref		
b	0.170	0.200	0.270	0.007	0.008	0.011
c	0.11	0.15	0.23	0.004	0.006	0.009
e	0.50 BSC.			0.020 BSC.		
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 Ref			0.063 Ref		
S	0.20	-	-	0.008	-	-

REGISTER DESCRIPTION

General Control Register

General Control Register				
Index	**Name**	**Bits**	**Description**	
00h	**REGBK**	**7:0**	**Default : 0x00**	**Access : R/W**
	XTAL_OK (RO)	7	Crystal ready.	
	MCU_SEL (RO)	6	0: Embedded MCU. 1: External serial bus interface.	
	-	5:4	Reserved.	
	AINC	3	Serial bus address auto Increase. 0: Enable. 1: Disable.	
	-	2	Reserved.	
	REGBK[1:0]	1:0	Register Bank Select. 00: Register of scaler. 01: Register of ADC/ACE/MCU. 10: Register of Video Decoder Front End (VFE). 11: Register of Video Decoder 2D Comb Filter (VCF).	
01h ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

Scaler Register (Bank = 00, Registers 01h ~ 9Fh)

Scaler Register (Bank=00, Registers 01h ~ 9Fh)				
Index	**Name**	**Bits**	**Description**	
01h	**DBFC**	**7:0**	**Default : 0x80**	**Access : R/W**
	-	7:3	Reserved.	
	DBL[1:0]	2:1	Double Buffer Load. 00: Keep old register value. 01: Load new data (auto reset to 00 when load finish). 10: Automatically load data at VSYNC blanking. 11: Reserved.	
	DB_EN	0	Double Buffer Enable. 0: Disable. 1: Enable.	
02h	**ISELECT**	**7:0**	**Default : 0x00**	**Access : R/W**
	NIS	7	No Input Source. 0: Input source active. 1: Input source inactive, output is free-run.	
	STYPE[1:0]	6:5	Input Sync Type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	COMP	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.	
	ICS	3	Input Color Space. 0: RGB. 1: YCbCr.	
	IHSU	2	Input Sync Usage. When EXTVD=0: 0: Use HSYNC to perform mode detection, HSOUT from ADC to sample pixel. 1: Use HSYNC only. When EXTVD=1: 0: Normal. 1: Output black at blanking.	
	BYPASSMD	1	By-Pass Mode for interlace-input-interlace-output.	
	EXTVD	0	0: Select analog input (CVBS/S-Video/RGB/YCbCr). 1: Select digital input (CCIR656).	
03h	**IPCTRL2**	**7:0**	**Default : 0x18**	**Access : R/W**
	VDS_EN	7	Input data double sample In CCIR input mode, 0: for horizontal output resolution less than 720 pixels. 1: for horizontal output resolution more than 720 pixels. In analog input mode, 0: half sample of input data. 1: original sample of input data.	
	VDS_MTHD	6	Input data double sample Method. 0: Using average. 1: Using advance GT filter.	
	IVDS	5	Input VSYNC Delay Select. 0: Delay 1/4 input HSYNC (recommended). 1: No delay.	
	HES	4	Input HSYNC reference Edge Select. 0: From HSYNC leading edge, default value. 1: From HSYNC tailing edge.	
	VES	3	Input VSYNC reference Edge Select. 0: From VSYNC leading edge, default value. 1: From VSYNC tailing edge.	
	ESLS	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.	
	VWRP	1	Input image Vertical Wrap. 0: Disable. 1: Enable.	
	HWRP	0	Input image Horizontal Wrap. 0: Disable. 1: Enable.	
04h	**ISCTRL**	**7:0**	**Default : 0x10**	**Access : R/W**

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	DDE	7	Direct DE mode for CCIR input. 0: Disable direct DE. 1: Enable direct DE.	
	DEGR[2:0]	6:4	DE or HSYNC post Glitch removal Range.	
	HSFL	3	Input HSYNC Filter. 0: Filter off. 1: Filter on.	
	ISSM	2	Input Sync Sample Mode. 0: Normal. 1: Glitch-removal.	
	MVD_SEL	1:0	MVD mode Select 0: CVBS. 1: S-Video. 2: YCbCr. 3: RGB.	
05h	**SPRVST_L**	**7:0**	**Default : 0x10**	**Access : R/W, DB**
	SPRVST[7:0]	7:0	Image vertical sample start point, count by input HSYNC (lower 8 bits).	
06h	**SPRVST_H**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:3	Reserved.	
	SPRVST[10:8]	2:0	Image vertical sample start point, count by input HSYNC (higher 3 bits).	
07h	**SPRHST_L**	**7:0**	**Default : 0x01**	**Access : R/W, DB**
	SPRHST[7:0]	7:0	Image horizontal sample start point, count by input dot clock (higher 8 bits).	
08h	**SPRHST_H**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:3	Reserved.	
	SPRGST[10:8]	2:0	Image horizontal sample start point, count by input dot clock (lower 3 bits).	
09h	**SPRVDC_L**	**7:0**	**Default : 0x10**	**Access : R/W, DB**
	SPRVDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line; lower 8 bits).	
0Ah	**SPRVDC_H**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRVDC[10:8]	2:0	Image vertical resolution (vertical display enable area count by line; higher 3 bits).	
0Bh	**SPRHDC_L**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRHDC[7:0]	7:0	Image horizontal resolution (horizontal display enable area count by pixel; lower 8 bits).	
0Ch	**SPRHDC_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRHDC[10:8]	2:0	Image horizontal resolution (horizontal display enable area count by pixel; higher 3 bits).	
0Dh	**LYL**	**7:0**	**Default : 0x00**	**Access : R/W**

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	-	7:4	Reserved.	
	LYL[3:0]	3:0	Lock Y Line.	
0Eh	**INTLX**	**7:0**	**Default : 0x00**	**Access : -**
	ITU_EXT_FIELD	7	Using External FIELD for ITU interface. 0: Using EAV/SAV. 1: Using external FIELD.	
	ITU_EXT_HS	6	Using External HSYNC for ITU interface. 0: Using EAV/SAV. 1: Using external HSYNC.	
	ITU_EXT_VS	5	Using External VSYNC for ITU interface. 0: Using EAV/SAV. 1: Using external VSYNC.	
	VDOE	4	Video reference Edge (for non-standard signal).	
	INTLAC_LOCKAVG	3	Averaging Locking timing.	
	LHC_MD	2	Long Horizontal Counter Mode. 1: On. 0: Off.	
	-	1:0	Reserved.	
0Fh	**ASCTRL**	**7:0**	**Default : 0x90**	**Access : R/W**
	IVB (RO)	7	Input VSYNC Blanking status. 0: In display. 1: In blanking.	
	DLINE[2:0]	6:4	Line buffer read delay in number of lines.	
	INTLAC_MANSTD	3	NTSC/PAL Manual Mode	
	INTLAC_SETSTD	2	NTSC/PAL Setting in manual mode under run status. 0: NTSC. 1: PAL.	
	UNDER (RO)	1	Under run status.	
	OVER (RO)	0	Over run status.	
10h	**COCTRL1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	AVI_SEL	5	Analog Video Input Select. 0: PC. 1: Component analog video.	
	DLYV	4	Analog Delay line for component analog Video input. 0: Delay 1 line. 1: Do not delay.	
	CSC_MD	3	Composite SYNC Cut Mode. 0: Disable. 1: Enable.	
	EXVS	2	External VSYNC polarity (only used when COVS is 1). 0: Normal. 1: Invert.	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	COV_SEL	1	Coast VSYNC Select. 0: Internal VSEP. 1: External VSYNC.	
	CADC	0	Coast to ADC. 0: Disable. 1: Enable.	
11h	**COCTRL2**	**7:0**	**Default : 0x00**	**Access : R/W**
	COST[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. … 254: Coast start from 255 HSYNC leading edge. 255: Coast start from 256 HSYNC leading edge.	
12h	**COCTRL3**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEND[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value. … 254: Coast end at 255 HSYNC leading edge. 255: Coast end at 256 HSYNC leading edge.	
13h	**VFAC_OINI**	**7:0**	**Default: 0x00**	**Access : R/W**
	VFACOINI[7:0]	7:0	Vertical Factor Odd Initial value.	
14h	**VFAC_EINI**	**7:0**	**Default: 0x80**	**Access : R/W**
	VFACEINI[7:0]	7:0	Vertical Factor Even Initial value	
15h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
16h	**INTCTROL**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHG_HMD	7	Change H Mode for INT. 0: Only in leading/tailing of CHG period. 1: Every line generating INT pulse during CHG period.	
	-	6:4	Reserved.	
	IVSI	3	Input VSYNC interrupt generated by: 0: Leading edge. 1: Tailing edge.	
	OVSI	2	Output VSYNC interrupt generated by: 0: Leading edge. 1: Tailing edge.	
	TRGC	1	Trigger Condition. 0: Active low for level trigger/tailing edge trigger. 1: Active high for level trigger/leading edge trigger.	
	INT_TRIG	0	Interrupt Trigger. 0: Generate an edge trigger interrupt. 1: Generate a level trigger interrupt.	
17h	**INTPULSE**	**7:0**	**Default : 0x0F**	**Access : R/W**
	INTPULSE[7:0]	7:0	Interrupt Pulse width by reference clock.	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
18h	**INTSTA**	**7:0**	**Default : 0x00**	**Access : R/W**
	INTSTA[7:0]	7:0	Interrupt Status byte A. Bit 7: MVD input NOT “no signal”. Bit 6: MVD “HSYNC lock”. Bit 5: MVD NOT “no color”. Bit 4: MVD degree error. Bit 3: MVD input “no signal”. Bit 2: MVD NOT “HSYNC lock”. Bit 1: MVD “no color”. Bit 0: MVD HSYNC change.	
19h	**INTENA**	**7:0**	**Default : 0x00**	**Access : R/W**
	INTENA[7:0]	7:0	Interrupt Enable control byte A. 0: Disable interrupt. 1: Enable interrupt.	
1Ah	**INTSTB**	**7:0**	**Default : 0x00**	**Access : R/W**
	INTSTB[7:0]	7:0	Interrupt Status byte B. Bit 7: MCU D2B interrupt 2. Bit 6: MCU D2B interrupt 1. Bit 5: MCU D2B interrupt 0. Bit 4: MVD CC interrupt. Bit 3: MVD SECAM detect. Bit 2: MVD PAL switch error. Bit 1: MVD “ADC7_0ACT”. Bit 0: MVD NOT “ADC7_0ACT”.	
1Bh	**INTENB**	**7:0**	**Default : 0x00**	**Access : R/C**
	INTENB[7:0]	7:0	Interrupt Enable control byte B. 0: Disable interrupt. 1: Enable interrupt.	
1Ch	**INTSTC**	**7:0**	**Default : 0x00**	**Access : R/W**
	INTSTC[7:0]	7:0	Interrupt Status byte C. Bit 7: Output VSYNC interrupt. Bit 6: Input VSYNC interrupt. Bit 5: ATG ready interrupt. Bit 4: ATP ready interrupt. Bit 3: ATS ready interrupt. Bit 2: MVD probe ready interrupt. Bit 1: MCU D2B interrupt 4. Bit 0: MCU D2B interrupt 3.	
1Dh	**INTENC**	**7:0**	**Default : 0x00**	**Access : R/C**
	INTENC[7:0]	7:0	Interrupt Enable control byte C. 0: Disable interrupt. 1: Enable interrupt.	
1Eh	**INTSTD**	**7:0**	**Default : 0x00**	**Access : R/W**

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	INTSTD[7:0]	7:0	Interrupt Status byte D. Bit 7: WDT interrupt. Bit 6: Keypad wake-up interrupt. Bit 5: Jitter interrupt. Bit 4: Horizontal total change interrupt. Bit 3: Vertical total change interrupt. Bit 2: Horizontal lost count interrupt. Bit 1: Vertical lost count interrupt. Bit 0: Standard change interrupt.	
1Fh	**INTEND**	**7:0**	**Default : 0x00**	**Access : R/C**
	INTEND[7:0]	7:0	Interrupt Enable control byte D. 0: Disable interrupt. 1: Enable interrupt.	
20h ~ 21h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
22h	**MPL_M**	**7:0**	**Default : 0x6F**	**Access : R/W**
	MP_ICTRL[2:0]	7:5	Charge pump current set.	
	MPL_M[4:0]	4:0	MPLL divider ratio setting.	
23h	**OPL_CTL0**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7:6	Reserved.	
	SSC_EN	6	Output PLL spread spectrum. 0: Disable. 1: Enable.	
	SD_MD	5	Output PLL spread spectrum Mode. 0: Normal. 1: Reverse for mode 1.	
	-	4:0	Reserved.	
24h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
25h	**OPL_SET0**	**7:0**	**Default : 0x44**	**Access : R/W, DB**
	OPL_SET[7:0]	7:0	Output PLL Set.	
26h	**OPL_SET1**	**7:0**	**Default : 0x55**	**Access : R/W, DB**
	OPL_SET[15:8]	7:0	See description for OPL_SET [7:0].	
27h	**OPL_SET2**	**7:0**	**Default : 0x24**	**Access : R/W, DB**
	OPL_SET [23:16]	7:0	See description for OPL_SET [7:0].	
28h	**OPL_STEP0**	**7:0**	**Default : 0x20**	**Access : R/W, DB**
	OPL_STEP[7:0]	7:0	Output PLL spread spectrum Step.	
29h	**OPL_STEP1**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7	Reserved.	
	-	6	Reserved.	
	-	5	Reserved.	
	-	4:3	Reserved.	
	OPL_STEP[10:8]	2:0	See description for OPL_STEP[7:0].	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
2Ah	**OPL_SPAN**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	OPL_SPAN[7:0]	7:0	Output PLL spread spectrum Span.	
2Bh	**OPL_SPAN**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	READ_FRAME	7	0: OPL_SET stores line-based value. 1: OPL_SET stores frame-based value.	
	OPL_SPAN[14:8]	6:0	See description for OPL_SPAN[7:0].	
2Ch ~ 2Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
30h	**HSR_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSR [7:0]	7:0	Horizontal Scaling ratio (20 bits fraction) for scaling down 1/2^20 to (2^20-1)/2^20 (lower 8 bits).	
31h	**HSR_M**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSR[15:8]	7:0	Horizontal Scaling ratio (20 bits fraction) for scaling down 1/2^20 to (2^20-1)/2^20 (middle 8 bits).	
32h	**HSR_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_EN	7	Horizontal Scaling Enable. 0: Disable. 1: Enable.	
	CBILINEAR_EN	6	Complemental Bi-Linear Enable.	
	FORCEBICOLOR	5	0: Chrominance using same setting as Luminance defined by CBILINEAR. 1: Chrominance always using bi-linear algorithm.	
	-	4	Reserved.	
	HSR[19:16]	3:0	Horizontal Scaling Ratio (20 bits fraction) for scaling down 1/2^20 to (2^20-1)/2^20 (higher 8 bits).	
33h	**VSR_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSR[7:0]	7:0	Vertical Scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999 (lower 8 bits). xx.xxxxxxxxxxxxxxxxxxx	
34h	**VSR_M**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSR[15:8]	7:0	Vertical Scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999 (middle 8 bits). xx.xxxxxxxxxxxxxxxxxxx	
35h	**VSR_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_EN	7	Vertical Scaling Enable. 0: Disable. 1: Enable.	
	VSM_SEL	6	Vertical Scaling Method Select. 0: Original. 1: New.	
	VSR[21:16]	5:0	Vertical Scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999 (higher 8 bits). xx.xxxxxxxxxxxxxxxxxxx	
36h	**VDSUSG**	**7:0**	**Default: 0x00**	**Access : R/W**

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	LBF_INCLK	7	Line-Buffer using Input Clock.	
	LBF_OUTCLK	6	Line-Buffer using Output Clock.	
	LBF_LIVE	5	Line-Buffer always Live.	
	OUTCLK_DIV3	4	Output Clock is 1/3 frequency of OPLL output.	
	EN_OFST	3	Enable Offset for even/odd scaling.	
	OFST_INV	2	Offset Inverting for even/odd scaling.	
	LBFCLK_DIV2	1	Line-Buffer Clock frequency is divided by 2.	
	VSD_DITH_EN	0	VSD Dither Enable.	
37h	**DIRSCAL_CTL**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GOAL2_SEL	2	Goal2 Select.	
	DITH_ON	1	Dithering control. 0: Off. 1: On.	
	DIRSCAL_EN	0	Function Enable.	
38h	**NLDTI**	**7:0**	**Default : 0x00**	**Access : R/W**
	NL_EN	7	Non-Linear scaling Enable.	
	NLSIO[6:0]	6:0	Non-Linear Scaling section Initial Offset.	
39h	**NLDT0**	**7:0**	**Default : 0x00**	**Access : R/W**
	NLIOS	7	Non-Linear scaling section Initial Offset Sign. 0: Positive value. 1: Negative value.	
	NLDT0[6:0]	6:0	Non-Linear Scaling Delta for Section 0, bit 7 is sign bit.	
3Ah	**NLDT1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved	
	NLDT1[6:0]	6:0	Non-Linear scaling Delta for Section 1, bit 7 is sign bit.	
3Bh	**NLDC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	NLDC0[7:0]	7:0	Non-Linear scaling section 0 Dot Count/2.	
3Ch	**NLDC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	NLDC1[7:0]	7:0	Non-Linear scaling section 1 Dot Count/2.	
3Dh	**NLDC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	NLDC2[7:0]	7:0	Non-Linear scaling section 2 Dot Count/2.	
3Eh	**DIRSCAL_TH1**	**7:0**	**Default: 0x80**	**Access : R/W**
	DETTH[7:0]	7:0	Threshold of maximum value for detection	
3Fh	**DIRSCAL_TH2**	**7:0**	**Default: 0x80**	**Access : R/W**
	PCTTH[7:0]	7:0	Threshold of maximum value for protection	
40h	**VFDEST_L**	**7:0**	**Default : 0x01**	**Access : R/W**
	VFDEST[7:0]	7:0	Output frame DE Vertical Start (lower 8 bits).	
41h	**DEVST_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	VFDEST[10:8]	2:0	Output frame DE Vertical Start (higher 3 bits).	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
42h	**HFDEST_L**	**7:0**	**Default : 0x03**	**Access : R/W**
	HFDEST[7:0]	7:0	Output frame DE Horizontal Start (lower 8 bits).	
43h	**HFDEST_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HFDEST[10:8]	2:0	Output frame DE Horizontal Start (higher 3 bits).	
44h	**VFDEEND_L**	**7:0**	**Default : 0xEA**	**Access : R/W**
	VFDEEND[7:0]	7:0	Output frame DE Vertical END (lower 8 bits).	
45h	**VFDEEND_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DEVEND[10:8]	2:0	Output frame DE Vertical END (higher 3 bits).	
46h	**HFDEEND_L**	**7:0**	**Default : 0xE0**	**Access : R/W**
	HFDEEND[7:0]	7:0	Output frame DE Horizontal END (lower 8 bits).	
47h	**HFDEEND_H**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	HFDEEND[10:8]	2:0	Output frame DE Horizontal END (higher 3 bits).	
48h	**SIHST_L**	**7:0**	**Default : 0x01**	**Access : R/W**
	SIHST[7:0]	7:0	Scaling Image window Horizontal Start (lower 8 bits).	
49h	**SIHST_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SIHST[10:8]	2:0	Scaling Image window Horizontal Start (higher 3 bits).	
4Ah	**SIVEND_L**	**7:0**	**Default : 0xEA**	**Access : R/W**
	SIVEND[7:0]	7:0	Scaling Image window Vertical END (lower 8 bits).	
4Bh	**SIVEND_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SIVEND[10:8]	2:0	Scaling Image window Vertical END (higher 3 bits).	
4Ch	**SIHEND_L**	**7:0**	**Default : 0xEA**	**Access : R/W**
	SIHEND[7:0]	7:0	Scaling Image window Horizontal END (lower 8 bits).	
4Dh	**SIHEND_H**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	SIHEND[10:8]	2:0	Scaling Image window Horizontal END (higher 3 bits).	
4Eh	**VDTOT_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDTOT[7:0]	7:0	Output Vertical Total (lower 8 bits).	
4Fh	**VDTOT_H**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	VDTOT[10:8]	2:0	Output Vertical Total (higher 3 bits).	
50h	**VSST_L**	**7:0**	**Default : 0xEA**	**Access : R/W**
	VSST[7:0]	7:0	Output VSYNC start (lower 8 bits).	
51h	**VSST_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	VSRU	3	VSYNC Register Usage. 0: Registers 20h – 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No signal VSYNC. Registers 22h and 23h are used to define minimum H total.	
	VSST[10:8]	2:0	Output VSYNC start (higher 3 bits).	
52h	**VSEND_L**	**7:0**	**Default : 0x06**	**Access : R/W**
	VSEND[7:0]	7:0	Output VSYNC END (lower 8 bits).	
53h	**VSEND_H**	**7:0**	**Default : 0x00**	**Access : R/W DB**
	-	7:3	Reserved.	
	VSEND[10:8]	2:0	Output VSYNC END (higher 3 bits).	
54h	**HDTOT_L**	**7:0**	**Default : 0x3C**	**Access : R/W DB**
	HDTOT[7:0]	7:0	Output Horizontal Total (lower 8 bits).	
55h	**HDTOT_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HDTOT[10:8]	2:0	Output Horizontal Total (higher 3 bits).	
56h	**HSEND**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSEND[7:0]	7:0	Output HSYNC END (lower 8 bits).	
57h	**OSCTRL1**	**7:0**	**Default : 0x4C**	**Access : R/W**
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x50 – 0x53).	
	LCM	6	Frame Lock Mode. 0: Mode 0. 1: Mode 1.	
	HRSM	5	HSYNC Remove Mode. 0: Normal. 1: Remove HSYNC.	
	-	4:3	Reserved.	
	Scal_1	2	Scaling range add 1.	
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.	
	CTRL	0	ATCTRL function enable. 0: Disable. 1: Enable.	
58h	**BRIGHTNESS_EN**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BRI_EN	0	Brightness function Enable. 0: Disable. 1: Enable.	
59h	**BRI_R**	**7:0**	**Default : 0x80**	**Access : R/W**
	BRI_R[7:0]	7:0	Brightness coefficient–Red color.	
5Ah	**BRI_G**	**7:0**	**Default : 0x80**	**Access : R/W**

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	BRI_G[7:0]	7:0	Brightness coefficient–Green color.	
5Bh	**BRI_B**	**7:0**	**Default : 0x80**	**Access : R/W**
	BRI_B[7:0]	7:0	Brightness coefficient–Blue color.	
5Ch	**FRAME_COLOR_1**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCG[4:3]	7:6	Frame Color G[4:3].	
	FCB[7:3]	5:1	Frame Color B[7:3].	
	FC_EN	0	Frame Color Enable. 0: Diable. 1: Enable.	
5Dh	**FRAME_COLOR_2**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCR[7:3]	7:3	Frame Color R[7:3].	
	FCG[7:5]	2:0	Frame Color G[7:5].	
5Eh	**PATTERN**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXT_OSD	7	EXT OSD pin as GPIO.	
	EXT_VD	6	EXT VD pin as GPIO.	
	-	5:3	Reserved.	
	PTNWT	2	Pattern White.	
	PTNBLK	1	Pattern Black.	
	PTNRVS	0	Pattern Reverse.	
5Fh	**EXT_OSD_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTOSD_EN	7	External OSD function Enable. 0: Diable. 1: Enable.	
	DATEXTMD[1:0]	6:5	Data Extend Mode.	
	CKEY_EN	4	Color Key Enable. 0: Disable. 1: Enable.	
	INVCKEY_EN	3	Inverse Color Key Enable. 0: Diable. 1: Enable.	
	R_KEY	2	R color Key selected.	
	G_KEY	1	G color Key selected.	
	B_KEY	0	B color Key selected.	
60h	**DITHCTRL**	**7:0**	**Default : 0x02**	**Access : R/W**
	DITHG[1:0]	7:6	Dither coefficient for G channel.	
	DITHB[1:0]	5:4	Dither coefficient for B channel.	
	SROT	3	Spatial coefficient Rotate. 0: Disable. 1: Enable.	
	TROT	2	Temporal coefficient Rotate. 0: Disable. 1: Enable.	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	OBN	1	Output Bits Number 0: 8-bit output. 1: 6-bit output (power on default value).	
	DITH	0	Dither function. 0: Off. 1: On.	
61h	**DITHCOEF**	**7:0**	**Default : 0x2D**	**Access : R/W**
	TL[1:0]	7:6	Top-Left dither coefficient.	
	TR[1:0]	5:4	Top-Right dither coefficient.	
	BL[1:0]	3:2	Bottom-Left dither coefficient.	
	BR[1:0]	1:0	Bottom-Right dither coefficient.	
62h	**DITHCTL1**	**7:0**	**Default : 0x00**	**Access : R/W**
	PSRD	7	Pseudo Random, resets every 4 frames. 0: Enable. 1: Disable.	
	ND_MD	6	Noise Dithering Method.	
	AUTO_DTH	5	Auto Dither.	
	PSDO_EN	4	Pseudo Enable. 0: Disable. 1: Enable.	
	DTH_MNUS	3	Dither Minus.	
	ABM[2:0]	2:0	Alpha Blending Mode. 000: No alpha blending. 001: Background alpha blending. 010: Foreground alpha blending. 011: Color key alpha blending. 100: Not color key alpha blending. 101: Entire OSD alpha blending. 11x: Reserved.	
63h	**OSD_CTL**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKIND[3:0]	7:4	Color Index of Color Key. 0000: Color index 0. 0001: Color index 1. … … 1111: Color index 15. When OSD register 0x10[7]=1, OSD is not backward compatible. When OSD register 0x10[7]=0, OSD is backward compatible. When 8-color palette is selected, only CKIND[2:0] are used. When 16-color palette is selected, OSD0xE0 bit[6] is color key bit[3] instead of using CKIND[3].	
	NEW_BLND_MTHD	3	New Blending Level. 0: Original blending level (BLENDL=000 means 0% transparency). 1: New blending level (BLENDL=000 means 12.5% transparency).	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	OSD_BLND_MD	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency. 011: 50.0%% transparency. 100: 62.5% transparency. 101: 75.0% transparency. 110: 87.5% transparency. 111: 100% transparency.	
64h	**CM11_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11 (lower 8 bits).	
65h	**CM11_H**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	Color Matrix Coefficient 11 (higher 5 bits).	
66h	**CM12_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12 (lower 8 bits).	
67h	**CM12_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	Color Matrix Coefficient 12 (higher 5 bits).	
68h	**CM13_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13 (lower 8 bits).	
69h	**CM13_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	Color Matrix Coefficient 13 (higher 5 bits).	
6Ah	**CM21_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21 (lower 8 bits).	
6Bh	**CM21_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	Color Matrix Coefficient 21 (higher 5 bits).	
6Ch	**CM22_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22 (lower 8 bits).	
6Dh	**CM22_H**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	Color Matrix Coefficient 22 (higher 5 bits).	
6Eh	**CM23_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23 (lower 8 bits).	
6Fh	**CM23_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	Color Matrix Coefficient 23 (higher 5 bits).	
70h	**CM31_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31 (lower 8 bits).	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
71h	**CM31_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	Color Matrix Coefficient 31 (higher 5 bits).	
72h	**CM32_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32 (lower 8 bits).	
73h	**CM32_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	Color Matrix Coefficient 32 (higher 5 bits).	
74h	**CM33_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33 (lower 8 bits).	
75h	**CM33_H**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	Color Matrix Coefficient 33 (higher 5 bits).	
76h	**COL_MATRIX_CTL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.	
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.	
77h	**FBL_CTL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved	
	ODDF	3	Shift Odd Field. 0: Shift even field. 1: Shift odd field.	
	SLN[2:0]	2:0	Shift Line Number. 000: Shift 0 line between odd and even fields. 001: Shift 1 line between odd and even fields. 010: Shift 2 line between odd and even fields. 011: Shift 3 line between odd and even fields. 1xx: Shift 4 line between odd and even fields.	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
78h	**LCK_VCNT_L**	**7:0**	**Default : -**	**Access : RO**
	LCK_VCNT[7:0]	7:0	Lock V total low byte [7:0].	
79h	**LCK_VCNT_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWCH_STS	7	Switch Status.	
	-	6:3	Reserved.	
	LCK_VCNT[10:8]	2:0	Lock V total high byte [10:8].	
7Ah	**CAP_VCNT_L**	**7:0**	**Default : -**	**Access : RO**
	CAP_VCNT[7:0]	7:0	Cap V total low byte [7:0].	
7Bh	**CAP_VCNT_H**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	CAP_VCNT[10:8]	2:0	Cap V total high byte [10:8].	
7Ch	**CAP_HCNT_L**	**7:0**	**Default : -**	**Access : RO**
	CAP_HCNT[7:0]	7:0	Cap H total low byte [7:0].	
7Dh	**CAP_HCNT_H**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	CAP_HCNT[10:8]	2:0	Cap H total high byte [10:8].	
7Eh	**EST_VCNT_L**	**7:0**	**Default : -**	**Access : RO**
	EST_VCNT[7:0]	7:0	Est V total low byte [7:0].	
7Fh	**EST_VCNT_H**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	EST_VCNT[10:8]	2:0	Est V total high byte [10:8].	
80h	**EST_HCNT_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EST_HCNT[7:0]	7:0	Est H total low byte [7:0].	
81h	**EST_HCNT_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	EST_HCNT[10:8]	2:0	Est H total low byte [10:8].	
82h	**SSC_TLRN**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSC_TLRN[7:0]	7:0	SSC Tolerance.	
83h	**Delta_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	DELTA[7:0]	2:0	Delta[7:0].	
84h	**Delta_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DELTA[12:8]	4:0	Delta[12:8].	
85h	**SSC_SHIFT**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSC_SHIFT[7:0]	7:0	SSC Shift.	
86h	**FNTN_TST**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MSK_SHRT_LN_CLK	5	Mask the Clock when in Short Line.	
	-	4	Reserved.	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	SYNC_GATE_MD	3	Mask HYSNC and Clock Mode.	
	RB_SWAP	2	Output channel RB Swap.	
	LM_SWAP_6	1	Output Channel MSB LSB Swap in 6-bit bus mode.	
	LM_SWAP_8	0	Output Channel MSB LSB Swap in 8-bit bus mode.	
87h	**DEBUG**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	EOCK	6	Select External ODCLK.	
	-	5:4	Reserved.	
	PTEN	3	PLL Test register protect bit Enable. 0: Disable. 1: Enable.	
	-	2:0	Reserved.	
88h	**SL_CNTRL_1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LIM_HS	5	Limit HSYNC period enable.	
	-	4:3	Reserved.	
	INT_CAP_EN	2	Interlace Capture Enable.	
	SHLN_FLD	1	Select Short Line Field.	
	FRZ_SHLN	0	Stop Short Line Update.	
89h	**SL_TUNE _1**	**7:0**	**Default : 0x70**	**Access : R/W**
	TNCOEF	7:5	Tune Coefficient.	
	LCK_THRHD	4:0	Lock Threshold.	
8Ah	**SL_TUNE_2**	**7:0**	**Default : 0x00**	**Access : R/W**
	LMT_D5D6D7_H	7:0	Limit PLL_SET High byte.	
8Bh	**SL_TUNE_3**	**7:0**	**Default : 0xC0**	**Access : R/W**
	LMT_D5D6D7_L	7:0	Limit PLL_SET Low byte.	
8Ch	**TARGET_SL_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	TARGET_SL_L	7:0	Target Short Line Low byte.	
8Dh	**TARGET_SL_H**	**7:0**	**Default : 0x01**	**Access : R/W**
	TARGET_SL_H	7:0	Target Short Line High byte.	
8Eh ~ 8Fh	**-**	**7:0**	**Default : -**	**Access : RO**
	-		Reserved.	
90h	**GAMMA_EN**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ADR_INC_EN	1	Address Increase Enable. 0: Disable. 1: Enable.	
	GAMMA_EN	0	Gamma Enable. 0: Disable. 1: Enable.	

Scaler Register (Bank=00, Registers 01h ~ 9Fh)				
Index	**Name**	**Bits**	**Description**	
91h	**GAMMA_ADR_PORT**	**7:0**	**Default : 0x00**	**Access : R/W**
	GMA_ADR_PORT[7:0]	7:0	Gamma Address Port [7:0].	
92h	**GAMMA_DAT_PORT**	**7:0**	**Default : 0x00**	**Access : R/W**
	GMA_DAT_PORT[7:0]	7:0	Gamma Data Port [7:0].	
93h	**R_BIAS**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_BIAS[7:0]	7:0	DC level in R channel positive part.	
94h	**R_RATIO**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_RATIO[7:0]	7:0	Ratio in R channel positive part.	
95h	**G_BIAS**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_BIAS[7:0]	7:0	DC level in G channel positive part.	
96h	**G_RATIO**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_RATIO[7:0]	7:0	Ratio in G channel positive part.	
97h	**B_BIAS**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_BIAS[7:0]	7:0	DC level in B channel positive part.	
98h	**B_RATIO**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_RATIO[7:0]	7:0	Ratio in B channel positive part.	
99h	**R_BIASN**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_BIASN[7:0]	7:0	Dc level in R channel negative part.	
9Ah	**R_RATION**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_RATION[7:0]	7:0	Ratio in R channel negative part.	
9Bh	**G_BIASN**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_BIASN[7:0]	7:0	DC level in G channel negative part.	
9Ch	**G_RATION**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_RATION[7:0]	7:0	Ratio in G channel negative part.	
9Dh	**B_BIASN**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_BIASN[7:0]	7:0	DC level in B channel negative part.	
9Eh	**B_RATION**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_RATION[7:0]	7:0	Ratio in B channel negative part.	
9Fh	**-**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:0	Reserved.	

OSD Register (Bank = 00, Registers A0h ~ AAh)

OSD Register (Bank=00)				
Index	**Mnemonic**	**Bits**	**Description**	
A0h	**OSDIOA**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOSB_MD	7	OSD SRAM I/O Access Burst Mode. 0: Disable. 1: Enable.	

OSD Register (Bank=00)

Index	Mnemonic	Bits	Description	
	CLR	6	OSD Clear Bit (write only). 0: Normal. 1: Clear code with 00h, attribute with 00h.	
	-	5	Reserved.	
	RF	4	OSD RAM Font I/O Access. 0: Disable. 1: Enable.	
	DC	3	OSD Display Code I/O Access. 0: Disable. 1: Enable.	
	DA	2	OSD Display Attribute I/O Access. 0: Disable. 1: Enable.	
	ORBW_MD	1	OSD Register Burst Write Mode. 0: Disable. 1: Enable.	
	ORBR_MD	0	OSD Register Burst Read Mode. 0: Disable. 1: Enable.	
A1h	**OSDRA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	OSDRA	5:0	OSD Register Address Port.	
A2h	**OSDRD**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDRD	7:0	OSD Register Data Port.	
A3h	**OSDFA**	**7:0**	**Default : -**	**Access : WO**
	OSDFA	7:0	OSD RAM Font Address Port.	
A4h	**OSDFD**	**7:0**	**Default : -**	**Access : WO**
	OSDFD	7:0	OSD RAM Font Data Port.	
A5h	**DISPCA_L**	**7:0**	**Default : -**	**Access : WO**
	DISPCA[7:0]	7:0	OSD Display Code Address Port.	
A6h	**DISPCA_H**	**7:0**	**Default : -**	**Access : WO**
	-	7:3	Reserved.	
	DISPCA[10:8]	2:0	OSD Display Code Address Port.	
A7h	**DISPCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DISPCD[7:0]	7:0	OSD Display Code Data Port (When write access disabled, this port report display code data).	
A8h	**DISPAA_L**	**7:0**	**Default : -**	**Access : WO**
	DISPAA[7:0]	7:0	OSD Display Attribute Address port.	
A9h	**DISPAA_H**	**7:0**	**Default : -**	**Access : WO**
	-	7:3	Reserved.	
	DISPAA[10:8]	2:0	OSD Display Attribute Address port.	
AAh	**DISPAD**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Bank=00)

Index	Mnemonic	Bits	Description	
	DISPAD[7:0]	7:0	OSD Display Attribute Data Port (When write access disabled, this port report display attribute data).	
AEh	**DISPCA_CTL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DISPAD_RE[8]	6	When write access disabled, this bit report display attribute data (bit 8).	
	-	5	Reserved.	
	DISPCD_RE[8]	4	When write access disabled, this bit report display code data (bit 8).	
	-	3	Reserved.	
	INS_DATA	2	OSD Code/Attribute 9th bit Data (Code (A7h)/Attribute (AAh) Data Extend bit).	
	-	1	Reserved.	
	CA_NO_WRITE	0	OSD Display Code and Attribute Write disable.	
	OSD CODE (9th bit)			
	ITALIC	8	OSD Italic Control 0: Disable. 1: Enable. (Please refer AEh bit 0 INS_DATA)	
	OSD Attribute (8-Color Palette)			
	HALF_TRAN	8	OSD Half-transparency Control. 0: Disable. 1: Enable. (Please refer AEh[0]: INS_DATA and 42h[2]: ALF_TRANEN)	
	BLNK_CTRL	7	OSD Blink Control. 0: Disable. 1: Enable.	
	FGCLR[2:0]	6:4	OSD Foreground Color Select. 000: Color index 0. 001: Color index 1. … 111: Color index 7.	
	BDER_CTRL	3	OSD Character Border Control. 0: Disable. 1: Enable. (Please refer 42h[5] UNDERLINE_MD)	
	BGCLR[2:0]	2:0	OSD Background Color select. 000: color index 0. 001: color index 1. … 111: color index 7.	
	OSD Attribute (16 Color Palette)			

OSD Register (Bank=00)			
Index	**Mnemonic**	**Bits**	**Description**
	FGCLR[3:0]	7:4	OSD Foreground Color Select. 0000: color index 0. 0001: color index 1. … 1111: color index 15.
	BGCLR[3:0]	3:0	OSD Background Color Select. 0000: color index 0. 0001: color index 1. … 1111: color index 15.

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)				
Index	**Mnemonic**	**Bits**	**Description**	
01h	**OSDDBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DBL[1:0]	2:1	Double Buffer Load. 00: Keep old register value. 01: Load new data (auto reset to 00 when loading completes). 10: Automatically load data at VSYNC blanking. 11: Reserved.	
	DB_EN	0	Double Buffer Enable. 0: Disable. 1: Enable.	
02h	**OHSTA-L**	**7:0**	**Default : 0x00**	**Access : R/W**
	OHSTA[7:0]	7:0	OSD windows Horizontal Start position (pixel) (lower 8 bits).	
03h	**OHSTA-H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OHSTA[10:8]	2:0	OSD windows Horizontal Start position (higher 3 bits).	
04h	**OVSTA-L**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVSTA[7:0]	7:0	OSD windows Vertical Start position (line) (lower 8 bits).	
05h	**OVSTA-H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	OVSTA[9:8]	1:0	OSD windows Vertical Start position (higher 2 bits).	
06h	**OSDW**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	OSDW[5:0]	5:0	OSD windows Width (OSDW + 1 (column)), maximum 64 columns.	
07h	**OSDH**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	OSDH[5:0]	5:0	OSD windows Height (OSDH + 1 (row)), maximum 64 rows.	
08h	**OHSPA**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description	
	-	7:6	Reserved.	
	OHSPA[5:0]	5:0	OSD windows Horizontal Space start position (OHSPA + 1 (column)).	
09h	**OVSPA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OVSPA[4:0]	4:0	OSD windows Vertical Space start position (OVSPA + 1 (row)).	
0Ah	**OSPW**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSPW[7:0]	7:0	OSD Space Width (8 * OSPW (pixel)).	
0Bh	**OSPH**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSPH[7:0]	7:0	OSD Space Height (8 * OSPH (line)).	
0Ch	**IOSDC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVS[1:0]	7:6	OSD Vertical Scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels.	
	OHS[1:0]	5:4	OSD Horizontal Scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels.	
	-	3:1	Reserved.	
	MWIN	0	OSD Main Window display. 0: Off. 1: On.	
0Dh	**IOSDC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	BDC	5	OSD Character Border type select. 0: All direction font boundary (border). 1: Bottom-right direction font boundary (shadow).	
	BDW	4	OSD character Border Width control. 0: One pixel with for all scale. 1: Scale with OVS[1:0] and OHS[1:0].	
	-	3	Reserved.	
	BCLR[2:0]	2:0	OSD Border Color index. 000: color index 0. 001: color index 1. … 111: color index 7.	
0Eh	**IOSDC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SHALL	5	OSD Shadow with All Direction. 0: Shadow with Bottom-Right direction (shadow). 1: Shadow with all direction (border).	

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description	
	SDC	4	OSD Window Shadow Control. 0: Off. 1: On.	
	SCLR[3:0]	3:0	OSD window Shadow Color index. 0000: Color index 0. 0001: Color index 1. … 1111: Color index 15.	
0Fh	**OSHC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDSH[3:0]	7:4	OSD Shadow Height.	
	OSDSW[3:0]	3:0	OSD Shadow Width.	
10h	**IOSDC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	LINE_SHIFT_EN	7	OSD line shift Enable (Please refer 45h bit 4~2 LINE_SHIFT_VAL).	
	FIELD_POL	6	OSD line shift Field Polarity.	
	-	5	Reserved.	
	EN_M4C	4	4 Color Font Enable. 0: Disable. 1: Enable.	
	F16H	3	OSD font high control. 0: Font height is 18. 1: Font height is 16.	
	PEXT	2	OSD 16 color palette extent method. 0: Extend with palette bit 3. 1: Extend with 0.	
	TRANEN	1	OSD Transparency Enable. 0: No transparency. 1: Color index which hit OSD Color index for transparency[2:0] is transparent of 8 color palette/ Color index which hit OSD Color index for transparency[3:0] is transparent of 16 color palette. (Please refer 42h bit 3~0 OSD Color index for transparency.)	
	T16C	0	OSD 16 Color Palette select. 0: 8 color palette. 1: 16 color palette.	
12h	**OCBUFO**	**7:0**	**Default : 0x00**	**Access : R/W**
	CO_SEL	7	OSD Code buffer Offset Select. 0: Use OSDW[5:0] as offset. 1: Use OOFFSET[5:0] as offset.	
	-	6	Reserved.	
	OOFFSET[5:0]	5:0	OSD code buffer Offset Value.	
13h	**OSDBA-L**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDBA[7:0]	7:0	OSD code Base Address (lower 8 bits).	
14h	**OSDBA-H**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description	
	OSDBA[10:8]	2:0	OSD code Base Address (higher 3 bits) (Please refer 45h bit7 CCRAM608X2. When CCRAM608X2 = 0, OSDBA[10:0] is programming from 0 to 4BFh; when CCRAM608X2 = 1, OSDBA[9:0] is programming from 0 to 25fh and OSDBA[10] is programming to select low or high part code/attribute SRAM).	
15h	**GCCTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	GVS[1:0]	7:6	Gradually color Vertical Scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels.	
	GHS[1:0]	5:4	Gradually color Horizontal Scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels.	
	GRAD	3	Enable OSD Gradual color function. 0: Disable. 1: Enable.	
	ADC_PG	2	ADC Pattern Generator select. 0: Normal. 1: ADC.	
	-	1:0	Reserved.	
16h	**GRADCLR**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCLR	7	Gradual color by Frame Color. 0: Use RCLR, GCLR, BCLR as starting gradual color. 1: Use Frame Color as starting gradual color.	
	-	6	Reserved.	
	RCLR[1:0]	5:4	Red starting gradual Color. 00: Red color is 00h. 01: Red color is 55h. 10: Red color is AAh. 11: Red color is FFh.	
	GCLR[1:0]	3:2	Green starting gradual Color. 00: Green color is 00h. 01: Green color is 55h. 10: Green color is AAh. 11: Green color is FFh.	
	BCLR[1:0]	1:0	Blue starting gradual Color. 00: Blue color is 00h. 01: Blue color is 55h. 10: Blue color is AAh. 11: Blue color is FFh.	
17h	**HGRADCR**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description	
	SR	7	Sign bit of Red color. 0: Increase. 1: Decrease.	
	IRH	6	Inverse bit of Red color. 0: Normal. 1: Invert.	
	R_GRADH[5:0]	5:0	Increase/decrease value of Red color.	
18h	**HGRADCG**	**7:0**	**Default : 0x00**	**Access : R/W**
	SG	7	Sign bit of Green color. 0: Increase. 1: Decrease.	
	IGH	6	Inverse bit of Green color. 0: Normal. 1: Invert.	
	G_GRADH[5:0]	5:0	Increase/decrease value of Green color.	
19h	**HGRADCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	SB	7	Sign bit of Blue color. 0: Increase. 1: Decrease.	
	IBH	6	Inverse bit of Blue color. 0: Normal. 1: Invert.	
	B_GRADH[5:0]	5:0	Increase/decrease value of Blue color.	
1Ah	**HGRADSR**	**7:0**	**Default : 0x00**	**Access : R/W**
	HGRADSR[7:0]	7:0	Horizontal Gradual Step of Red color.	
1Bh	**HGRADSG**	**7:0**	**Default : 0x00**	**Access : R/W**
	HGRADSG[7:0]	7:0	Horizontal Gradual Step of Green color.	
1Ch	**HGRADSB**	**7:0**	**Default : 0x00**	**Access : R/W**
	HGRADSB[7:0]	7:0	Horizontal Gradual Step of Blue color.	
1Dh	**VGRADCR**	**7:0**	**Default : 0x00**	**Access : R/W**
	SR	7	Sign bit of Red color. 0: Increase. 1: Decrease.	
	IRV	6	Inverse bit of Red color. 0: Normal. 1: Invert.	
	R_GRADV[5:0]	5:0	Increase/decrease value of Red color.	
1Eh	**VGRADCG**	**7:0**	**Default : 0x00**	**Access : R/W**
	SG	7	Sign bit of Green color. 0: Increase. 1: Decrease.	
	IGV	6	Inverse bit of Green color. 0: Normal. 1: Invert.	

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description	
	G_GRADV[5:0]	5:0	Increase/Decrease value of Green color.	
1Fh	**VGRADCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	SB	7	Sign bit of Blue color. 0: Increase. 1: Decrease.	
	IBV	6	Inverse bit of Blue color. 0: Normal. 1: Invert.	
	B_GRADV[5:0]	5:0	Increase/decrease value of Blue color.	
20h	**VGRADSR**	**7:0**	**Default : 0x00**	**Access : R/W**
	VGRADSR[7:0]	7:0	Vertical Gradual Step of Red color.	
21h	**VGRADSG**	**7:0**	**Default : 0x00**	**Access : R/W**
	VGRADSG[7:0]	7:0	Vertical Gradual Step of Green color.	
22h	**VGRADSB**	**7:0**	**Default : 0x00**	**Access : R/W**
	VGRADSB[7:0]	7:0	Vertical Gradual Step of Blue color.	
23h ~ 25h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
26h	**TIMECTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FRG_EN	4	OSD Font Ram Gated Enable. 0: Disable. 1: Enable.	
	-	3:2	Reserved	
	VSTDLY	1	OSD Vertical Start Delay. 0: Normal. 1: Vertical Delay 1 line.	
	-	0	Reserved.	
27h	**OSDRTP**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RTPT	2	OSD Random Test Pattern Type. 0: RGB is the same. 1: RGB is different.	
	OSDRTP[1:0]	1:0	OSD Random Test Pattern. 00: Disable. 01: 1 random bit. 10: 2 random bit. 11: Reserved.	
OSD Color Palette when T16_C = 0				
28h	**CLR0R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR0R[7:0]	7:0	Red Color Index 0.	
29h	**CLR0G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR0G[7:0]	7:0	Green Color Index 0.	

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description	
2Ah	**CLR0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR0B[7:0]	7:0	Blue Color Index 0.	
2Bh	**CLR1R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR1R[7:0]	7:0	Red Color Index 1.	
2Ch	**CLR1G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR1G[7:0]	7:0	Green Color Index 1.	
2Dh	**CLR1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR1B[7:0]	7:0	Blue Color Index 1.	
2Eh	**CLR2R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR2R[7:0]	7:0	Red Color Index 2.	
2Fh	**CLR2G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR2G[7:0]	7:0	Green Color Index 2.	
30h	**CLR2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR2B[7:0]	7:0	Blue Color Index 2.	
31h	**CLR3R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR3R[7:0]	7:0	Red Color Index 3.	
32h	**CLR3G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR3G[7:0]	7:0	Green Color Index 3.	
33h	**CLR3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR3B[7:0]	7:0	Blue Color Index 3.	
34h	**CLR4R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR4R[7:0]	7:0	Red Color Index 4.	
35h	**CLR4G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR4G[7:0]	7:0	Green Color Index 4.	
36h	**CLR4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR4B[7:0]	7:0	Blue Color Index 4.	
37h	**CLR5R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR5R[7:0]	7:0	Red Color Index 5.	
38h	**CLR5G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR5G[7:0]	7:0	Green Color Index 5.	
39h	**CLR5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR5B[7:0]	7:0	Blue Color Index 5.	
3Ah	**CLR6R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR6R[7:0]	7:0	Red Color Index 6.	
3Bh	**CLR6G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR6G[7:0]	7:0	Green Color Index 6.	
3Ch	**CLR6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR6B[7:0]	7:0	Blue Color Index 6.	

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description	
3Dh	**CLR7R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR7R[7:0]	7:0	Red Color Index 7.	
3Eh	**CLR7G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR7G[7:0]	7:0	Green Color Index 7.	
3Fh	**CLR7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR7B[7:0]	7:0	Blue Color Index 7.	
OSD Color Palette when T16_C = 1 (16 color format: col[7:4], 4'b0 or col[7:4], {4{col[4]}})				
28h	**CLR0R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR0R[7:4]	7:4	Red Color Index 0.	
	CLR8R[3:0]	3:0	Red Color Index 8.	
29h	**CLR0G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR0G[7:4]	7:4	Green Color Index 0.	
	CLR8G[3:0]	3:0	Green Color Index 8.	
2Ah	**CLR0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR0B[7:4]	7:4	Blue Color Index 0.	
	CLR8B[3:0]	3:0	Blue Color Index 8.	
2Bh	**CLR1R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR1R[7:4]	7:4	Red Color Index 1.	
	CLR9R[3:0]	3:0	Red Color Index 9.	
2Ch	**CLR1G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR1G[7:4]	7:4	Green Color Index 1.	
	CLR9G[3:0]	3:0	Green Color Index 9.	
2Dh	**CLR1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR1B[7:4]	7:4	Blue Color Index 1.	
	CLR9B[3:0]	3:0	Blue Color Index 9.	
2Eh	**CLR2R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR2R[7:4]	7:4	Red Color Index 2.	
	CLR10R[3:0]	3:0	Red Color Index 10.	
2Fh	**CLR2G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR2G[7:4]	7:4	Green Color Index 2.	
	CLR10G[3:0]	3:0	Green Color Index 10.	
30h	**CLR2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR2B[7:4]	7:4	Blue Color Index 2.	
	CLR10B[3:0]	3:0	Blue Color Index 10.	
31h	**CLR3R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR3R[7:4]	7:4	Red Color Index 3.	
	CLR11R[3:0]	3:0	Red Color Index 11.	
32h	**CLR3G**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description	
	CLR3G[7:4]	7:4	Green Color Index 3.	
	CLR11G[3:0]	3:0	Green Color Index 11.	
33h	**CLR3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR3B[7:4]	7:4	Blue Color Index 3.	
	CLR11B[3:0]	3:0	Blue Color Index 11.	
34h	**CLR4R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR4R[7:4]	7:4	Red Color Index 4.	
	CLR12R[3:0]	3:0	Red Color Index 12.	
35h	**CLR4G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR4G[7:4]	7:4	Green Color Index 4.	
	CLR12G[3:0]	3:0	Green Color Index 12.	
36h	**CLR4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR4B[7:4]	7:4	Blue Color Index 4.	
	CLR12B[3:0]	3:0	Blue Color Index 12.	
37h	**CLR5R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR5R[7:4]	7:4	Red Color Index 5.	
	CLR13R[3:0]	3:0	Red Color Index 13.	
38h	**CLR5G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR5G[7:4]	7:4	Green Color Index 5.	
	CLR13G[3:0]	3:0	Green Color Index 13.	
39h	**CLR5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR5B[7:4]	7:4	Blue Color Index 5.	
	CLR13B[3:0]	3:0	Blue Color Index 13.	
3Ah	**CLR6R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR6R[7:4]	7:4	Red Color Index 6.	
	CLR14R[3:0]	3:0	Red Color Index 14.	
3Bh	**CLR6G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR6G[7:4]	7:4	Green Color Index 6.	
	CLR14G[3:0]	3:0	Green Color Index 14.	
3Ch	**CLR6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR6B[7:4]	7:4	Blue Color Index 6.	
	CLR14B[3:0]	3:0	Blue Color Index 14.	
3Dh	**CLR7R**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR7R[7:4]	7:4	Red Color Index 7.	
	CLR15R[3:0]	3:0	Red Color Index 15.	
3Eh	**CLR7G**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR7G[7:4]	7:4	Green Color Index 7.	
	CLR15G[3:0]	3:0	Green Color Index 15.	

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description	
3Fh	**CLR7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLR7B[7:4]	7:4	Blue Color Index 7.	
	CLR15B[3:0]	3:0	Blue Color Index 15.	
40h	**SCRLSPD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRLSPD[7:0]	7:0	OSD Scroll function speed (the numbers of VSYNC).	
41h	**SCRLLINE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCREN	7	OSD Scroll function Enable. 0: Disable. 1: Enable.	
	VSCR_FAST	6	Scroll at every VSYNC.	
	TRUC_EN	5	Truncate code/attribute Enable. 0: Disable. 1: Enable.	
	SCRLLINE[4:0]	4:0	OSD Scroll function (the numbers of scan lines per scroll).	
42h	**UNDERLINE**	**7:0**	**Default : 0x0F**	**Access : R/W**
	UNDERLINE_1	7	OSD Underline at last line.	
	UNDERLINE_2	6	OSD Underline at second last line.	
	UNDERLINE_MD	5	OSD Underline Mode enable (When this bit is asserted, OSD Attribute (8 Color) bit 3. (BDER) Character Boder Control change function to OSD Character Underline Control).	
	HALF_TRANEN	4	OSD Half-Transparency Enable (When this bit is asserted, OSD Attribute (8 Color) bit 9 (HALF_TRAN) is active.).	
	TRAN_INDEX[3:0]	3:0	OSD Color Index for Transparency (Define which color index is transparent).	
43h	**TRUNCATE**	**7:0**	**Default : 0x 1D**	**Access : R/W**
	TRUNCATENUM	7:0	OSD Truncate number (Please refer 45h bit7 CCRAM608X2. When CCRAM608X2=0, final row=(11'h4bf-TRUNCATENUM); when CCRAM608X2=1, final row=(11'h25f-TRUNCATENUM)).	
44h	**ITALIC**	**7:0**	**Default : 0x 00**	**Access : R/W**
	ITALIC_OFFSET	7:6	OSD Italic right shift Offset (00: 1, 01: 2, 10: 3, 11: 4 (pixel)).	
	ITALIC_1ST_LINE	5:4	OSD Italic start scan Line (00: 0, 01: 1, 10: 2, 11: 3 (line)).	
	ITALIC_STEP	3:2	OSD Italic left shift Step (00: 0.001, 01: 0.010, 10: 0.011, 11: 0.100 (pixel , binary)).	
	ITALIC_EN	1	OSD Italic function Enable. 0: Disable. 1: Enable.	
	-	0	Reserved.	
45h	**MISC_CTL**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCRAM608X2	7	OSD 2 608 code/attribute SRAM (When CCRAM608X2 = 0, there is one 1216 code/attribute SRAM for using; when CCRAM608X2 = 1, there are two 608 code/attribute SRAM for using.).	
	-	6:5	Reserved.	

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

Index	Mnemonic	Bits	Description	
	LINE_SHIFT_VAL[2:0]	4:2	OSD Line shift value (Line shift number, 000: 1, …, 111: 8).	
	CARHG_EN	1	OSD code/attribute high part ram gated Enable. 0: Disable. 1: Enable.	
	-	0	Reserved.	
46h	**OSD4CFFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD4CFFA[7:0]	7:0	OSD 4 Color Font RAM start Address (must be even number).	
47h ~ 49h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
4Ah	**OHVSTA-H**	**7:0**	**Default : 0x00**	**Access : RO**
	VSCR_OPT	7	Vscroll Option. 0: Original. 1: Fixed.	
	-	6	Reserved.	
	OVSTA[9:8]	5:4	OSD windows Vertical Start position (Read only).	
	-	3	Reserved.	
	OHSTA[10:8]	2:0	OSD windows Horizontal Start position. (Read only).	
4Bh ~ 4Ch	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
4Dh	**OSDBRI**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDBRI_EN	7	OSD Brightness Enable. 0: Disable. 1: Enable.	
	OSDBRI_DIR	6	OSD Brightness Control. 0: Add. 1: Subtract.	
	OSDBRI_VAL[5:0]	5:0	OSD Brightness Value.	
4Eh ~ 4Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
50h	**CODECLRDATA_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODECLRDATA[7:0]	7:0	OSD Code Clear Data.	
51h	**ATRCLRDATA_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATRCLRDAT[7:0]	7:0	OSD Attribute Clear Data (lower 8 bits).	
52h	**OSDCLRDATA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRCLRDAT[8]	4	OSD Attribute Clear Data.	
	-	3:1	Reserved.	
	CODECLRDAT[8]	0	OSD Code Clear Data.	
53h	**OSDCLRADR_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCLR_ADR[7:0]	7:0	OSD Clear Starting address (lower 8 bits).	
54h	**OSDCLRADR_H**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)				
Index	**Mnemonic**	**Bits**	**Description**	
	ATR1_CLREN	7	OSD Attribute High Clear Enable.	
	ATR0_CLREN	6	OSD Attribute Low Clear Enable.	
	CODE1_CLREN	5	OSD Code High Clear Enable.	
	CODE0_CLREN	4	OSD Code Low Clear Enable.	
	-	3:2	Reserved.	
	OSDCLR_ADR[9:8]	1:0	OSD Clear Starting Address.	
55h	**OSDCLR_OFST**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved	
	OSDCLR_OFST[6:0]	6:0	OSD Clear Offset.	
56h	**OSDCLR_WID**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OSDCLR_WID[6:0]	6:0	OSD Clear Width.	
57h	**OSDCLR_HIGT**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OSDCLR_HIGT[6:0]	6:0	OSD Clear Height.	
58h	**OSDCLR_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BLK_CLR_EN	0	OSD Block Clear Enable.	
59h ~ 9Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)

Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)				
Index	**Mnemonic**	**Bits**	**Description**	
00h	**Gamma_R00**	**7:0**	**Default : 0d00**	**Access : R/W**
	Gamma_R00	7:0	Gamma_table R00 value.	
01h	**Gamma_R01**	**7:0**	**Default : 0d07**	**Access : R/W**
	Gamma_R01	7:0	Gamma_table R01 value.	
02h	**Gamma_R02**	**7:0**	**Default : 0d15**	**Access : R/W**
	Gamma_R02	7:0	Gamma_table R02 value.	
03h	**Gamma_R03**	**7:0**	**Default : 0d23**	**Access : R/W**
	Gamma_R03	7:0	Gamma_table R03 value.	
04h	**Gamma_R04**	**7:0**	**Default : 0d31**	**Access : R/W**
	Gamma_R04	7:0	Gamma_table R04 value.	
05h	**Gamma_R05**	**7:0**	**Default : 0d39**	**Access : R/W**
	Gamma_R05	7:0	Gamma_table R05 value.	
06h	**Gamma_R06**	**7:0**	**Default : 0d47**	**Access : R/W**
	Gamma_R06	7:0	Gamma_table R06 value.	
07h	**Gamma_R07**	**7:0**	**Default : 0d55**	**Access : R/W**

Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)

Index	Mnemonic	Bits	Description	
	Gamma_R07	7:0	Gamma_table R07 value	
08h	**Gamma_R08**	**7:0**	**Default : 0d63**	**Access : R/W**
	Gamma_R08	7:0	Gamma_table R08 value.	
09h	**Gamma_R09**	**7:0**	**Default : 0d71**	**Access : R/W**
	Gamma_R09	7:0	Gamma_table R09 value.	
0Ah	**Gamma_R10**	**7:0**	**Default : 0d79**	**Access : R/W**
	Gamma_R10	7:0	Gamma_table R10 value.	
0Bh	**Gamma_R11**	**7:0**	**Default : 0d87**	**Access : R/W**
	Gamma_R11	7:0	Gamma_table R11 value.	
0Ch	**Gamma_R12**	**7:0**	**Default : 0d95**	**Access : R/W**
	Gamma_R12	7:0	Gamma_table R12 value.	
0Dh	**Gamma_R13**	**7:0**	**Default : 0d103**	**Access : R/W**
	Gamma_R13	7:0	Gamma_table R13 value.	
0Eh	**Gamma_R14**	**7:0**	**Default : 0d111**	**Access : R/W**
	Gamma_R14	7:0	Gamma_table R14 value.	
0Fh	**Gamma_R15**	**7:0**	**Default : 0d119**	**Access : R/W**
	Gamma_R15	7:0	Gamma_table R15 value.	
10h	**Gamma_R16**	**7:0**	**Default : 0d127**	**Access : R/W**
	Gamma_R16	7:0	Gamma_table R16 value.	
11h	**Gamma_R17**	**7:0**	**Default : 0d135**	**Access : R/W**
	Gamma_R17	7:0	Gamma_table R17 value.	
12h	**Gamma_R18**	**7:0**	**Default : 0d143**	**Access : R/W**
	Gamma_R18	7:0	Gamma_table R18 value.	
13h	**Gamma_R19**	**7:0**	**Default : 0d151**	**Access : R/W**
	Gamma_R49	7:0	Gamma_table R19 value.	
14h	**Gamma_R20**	**7:0**	**Default : 0d159**	**Access : R/W**
	Gamma_R20	7:0	Gamma_table R20 value.	
15h	**Gamma_R21**	**7:0**	**Default : 0d167**	**Access : R/W**
	Gamma_R21	7:0	Gamma_table R21 value.	
16h	**Gamma_R22**	**7:0**	**Default : 0d175**	**Access : R/W**
	Gamma_R22	7:0	Gamma_table R22 value.	
17h	**Gamma_R23**	**7:0**	**Default : 0d183**	**Access : R/W**
	Gamma_R23	7:0	Gamma_table R23 value.	
18h	**Gamma_R24**	**7:0**	**Default : 0d191**	**Access : R/W**
	Gamma_R24	7:0	Gamma_table R24 value.	
19h	**Gamma_R25**	**7:0**	**Default : 0d199**	**Access : R/W**
	Gamma_R25	7:0	Gamma_table R25 value.	
1Ah	**Gamma_R26**	**7:0**	**Default : 0d207**	**Access : R/W**
	Gamma_R26	7:0	Gamma_table R26 value.	

Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)				
Index	**Mnemonic**	**Bits**	**Description**	
1Bh	**Gamma_R27**	**7:0**	**Default : 0d215**	**Access : R/W**
	Gamma_R27	7:0	Gamma_table R27 value.	
1Ch	**Gamma_R28**	**7:0**	**Default : 0d223**	**Access : R/W**
	Gamma_R28	7:0	Gamma_table R28 value.	
1Dh	**Gamma_R29**	**7:0**	**Default : 0d232**	**Access : R/W**
	Gamma_R29	7:0	Gamma_table R29 value.	
1Eh	**Gamma_R30**	**7:0**	**Default : 0d239**	**Access : R/W**
	Gamma_R30	7:0	Gamma_table R30 value.	
1Fh	**Gamma_R31**	**7:0**	**Default : 0d247**	**Access : R/W**
	Gamma_R31	7:0	Gamma_table R31 value.	
20h	**Gamma_R32**	**7:0**	**Default : 0d255**	**Access : R/W**
	Gamma_R32	7:0	Gamma_table R32 value.	
21h	**Gamma_G00**	**7:0**	**Default : 0d00**	**Access : R/W**
	Gamma_G00	7:0	Gamma_table G00 value.	
22h	**Gamma_G01**	**7:0**	**Default : 0d07**	**Access : R/W**
	Gamma_G01	7:0	Gamma_table G01 value.	
23h	**Gamma_G02**	**7:0**	**Default : 0d15**	**Access : R/W**
	Gamma_G02	7:0	Gamma_table G02 value.	
24h	**Gamma_G03**	**7:0**	**Default : 0d23**	**Access : R/W**
	Gamma_G03	7:0	Gamma_table G03 value.	
25h	**Gamma_G04**	**7:0**	**Default : 0d31**	**Access : R/W**
	Gamma_G04	7:0	Gamma_table G04 value.	
26h	**Gamma_G05**	**7:0**	**Default : 0d39**	**Access : R/W**
	Gamma_G05	7:0	Gamma_table G05 value.	
27h	**Gamma_G06**	**7:0**	**Default : 0d47**	**Access : R/W**
	Gamma_G06	7:0	Gamma_table G06 value.	
28h	**Gamma_G07**	**7:0**	**Default : 0d55**	**Access : R/W**
	Gamma_G07	7:0	Gamma_table G07 value.	
29h	**Gamma_G08**	**7:0**	**Default : 0d63**	**Access : R/W**
	Gamma_G08	7:0	Gamma_table G08 value.	
2Ah	**Gamma_G09**	**7:0**	**Default : 0d71**	**Access : R/W**
	Gamma_G09	7:0	Gamma_table G09 value.	
2Bh	**Gamma_G10**	**7:0**	**Default : 0d79**	**Access : R/W**
	Gamma_G10	7:0	Gamma_table G10 value.	
2Ch	**Gamma_G11**	**7:0**	**Default : 0d87**	**Access : R/W**
	Gamma_G11	7:0	Gamma_table G11 value.	
2Dh	**Gamma_G12**	**7:0**	**Default : 0d95**	**Access : R/W**
	Gamma_G12	7:0	Gamma_table G12 value.	
2Eh	**Gamma_G13**	**7:0**	**Default : 0d103**	**Access : R/W**

Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)				
Index	**Mnemonic**	**Bits**	**Description**	
	Gamma_G13	7:0	Gamma_table G13 value.	
2Fh	**Gamma_G14**	**7:0**	**Default : 0d111**	**Access : R/W**
	Gamma_G14	7:0	Gamma_table G14 value.	
30h	**Gamma_G15**	**7:0**	**Default : 0d119**	**Access : R/W**
	Gamma_G15	7:0	Gamma_table G15 value.	
31h	**Gamma_G16**	**7:0**	**Default : 0d127**	**Access : R/W**
	Gamma_G16	7:0	Gamma_table G16 value.	
32h	**Gamma_G17**	**7:0**	**Default : 0d135**	**Access : R/W**
	Gamma_G17	7:0	Gamma_table G17 value.	
33h	**Gamma_G18**	**7:0**	**Default : 0d143**	**Access : R/W**
	Gamma_G18	7:0	Gamma_table G18 value.	
34h	**Gamma_G19**	**7:0**	**Default : 0d151**	**Access : R/W**
	Gamma_G49	7:0	Gamma_table G19 value.	
35h	**Gamma_G20**	**7:0**	**Default : 0d159**	**Access : R/W**
	Gamma_G20	7:0	Gamma_table G20 value.	
36h	**Gamma_G21**	**7:0**	**Default : 0d167**	**Access : R/W**
	Gamma_G21	7:0	Gamma_table G21 value.	
37h	**Gamma_G22**	**7:0**	**Default : 0d175**	**Access : R/W**
	Gamma_G22	7:0	Gamma_table G22 value.	
38h	**Gamma_G23**	**7:0**	**Default : 0d183**	**Access : R/W**
	Gamma_G23	7:0	Gamma_table G23 value.	
39h	**Gamma_G24**	**7:0**	**Default : 0d191**	**Access : R/W**
	Gamma_G24	7:0	Gamma_table G24 value.	
3Ah	**Gamma_G25**	**7:0**	**Default : 0d199**	**Access : R/W**
	Gamma_G25	7:0	Gamma_table G25 value.	
3Bh	**Gamma_G26**	**7:0**	**Default : 0d207**	**Access : R/W**
	Gamma_G26	7:0	Gamma_table G26 value.	
3Ch	**Gamma_G27**	**7:0**	**Default : 0d215**	**Access : R/W**
	Gamma_G27	7:0	Gamma_table G27 value.	
3Dh	**Gamma_G28**	**7:0**	**Default : 0d223**	**Access : R/W**
	Gamma_G28	7:0	Gamma_table G28 value.	
3Eh	**Gamma_G29**	**7:0**	**Default : 0d232**	**Access : R/W**
	Gamma_G29	7:0	Gamma_table G29 value.	
3Fh	**Gamma_G30**	**7:0**	**Default : 0d239**	**Access : R/W**
	Gamma_G30	7:0	Gamma_table G30 value.	
40h	**Gamma_G31**	**7:0**	**Default : 0d247**	**Access : R/W**
	Gamma_G31	7:0	Gamma_table G31 value.	
41h	**Gamma_G32**	**7:0**	**Default : 0d255**	**Access : R/W**
	Gamma_G32	7:0	Gamma_table G32 value.	

Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)				
Index	**Mnemonic**	**Bits**	**Description**	
42h	**Gamma_B00**	**7:0**	**Default : 0d00**	**Access : R/W**
	Gamma_B00	7:0	Gamma_table B00 value.	
43h	**Gamma_B01**	**7:0**	**Default : 0d07**	**Access : R/W**
	Gamma_B01	7:0	Gamma_table B01 value.	
44h	**Gamma_B02**	**7:0**	**Default : 0d15**	**Access : R/W**
	Gamma_B02	7:0	Gamma_table B02 value.	
45h	**Gamma_B03**	**7:0**	**Default : 0d23**	**Access : R/W**
	Gamma_B03	7:0	Gamma_table B03 value.	
46h	**Gamma_B04**	**7:0**	**Default : 0d31**	**Access : R/W**
	Gamma_B04	7:0	Gamma_table B04 value.	
47h	**Gamma_B05**	**7:0**	**Default : 0d39**	**Access : R/W**
	Gamma_B05	7:0	Gamma_table B05 value.	
48h	**Gamma_B06**	**7:0**	**Default : 0d47**	**Access : R/W**
	Gamma_B06	7:0	Gamma_table B06 value.	
49h	**Gamma_B07**	**7:0**	**Default : 0d55**	**Access : R/W**
	Gamma_B07	7:0	Gamma_table B07 value.	
4Ah	**Gamma_B08**	**7:0**	**Default : 0d63**	**Access : R/W**
	Gamma_B08	7:0	Gamma_table B08 value.	
4Bh	**Gamma_B09**	**7:0**	**Default : 0d71**	**Access : R/W**
	Gamma_B09	7:0	Gamma_table B09 value.	
4Ch	**Gamma_B10**	**7:0**	**Default : 0d79**	**Access : R/W**
	Gamma_B10	7:0	Gamma_table B10 value.	
4Dh	**Gamma_B11**	**7:0**	**Default : 0d87**	**Access : R/W**
	Gamma_B11	7:0	Gamma_table B11 value.	
4Eh	**Gamma_B12**	**7:0**	**Default : 0d95**	**Access : R/W**
	Gamma_B12	7:0	Gamma_table B12 value.	
4Fh	**Gamma_B13**	**7:0**	**Default : 0d103**	**Access : R/W**
	Gamma_B13	7:0	Gamma_table B13 value.	
50h	**Gamma_B14**	**7:0**	**Default : 0d111**	**Access : R/W**
	Gamma_B14	7:0	Gamma_table B14 value.	
51h	**Gamma_B15**	**7:0**	**Default : 0d119**	**Access : R/W**
	Gamma_B15	7:0	Gamma_table B15 value.	
52h	**Gamma_B16**	**7:0**	**Default : 0d127**	**Access : R/W**
	Gamma_B16	7:0	Gamma_table B16 value.	
53h	**Gamma_B17**	**7:0**	**Default : 0d135**	**Access : R/W**
	Gamma_B17	7:0	Gamma_table B17 value.	
54h	**Gamma_B18**	**7:0**	**Default : 0d143**	**Access : R/W**
	Gamma_B18	7:0	Gamma_table B18 value.	
55h	**Gamma_B19**	**7:0**	**Default : 0d151**	**Access : R/W**

Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)				
Index	**Mnemonic**	**Bits**	**Description**	
	Gamma_B49	7:0	Gamma_table B19 value.	
56h	**Gamma_B20**	**7:0**	**Default : 0d159**	**Access : R/W**
	Gamma_B20	7:0	Gamma_table B20 value.	
57h	**Gamma_B21**	**7:0**	**Default : 0d167**	**Access : R/W**
	Gamma_B21	7:0	Gamma_table B21 value.	
58h	**Gamma_B22**	**7:0**	**Default : 0d175**	**Access : R/W**
	Gamma_B22	7:0	Gamma_table B22 value.	
59h	**Gamma_B23**	**7:0**	**Default : 0d183**	**Access : R/W**
	Gamma_B23	7:0	Gamma_table B23 value.	
5Ah	**Gamma_B24**	**7:0**	**Default : 0d191**	**Access : R/W**
	Gamma_B24	7:0	Gamma_table B24 value.	
5Bh	**Gamma_B25**	**7:0**	**Default : 0d199**	**Access : R/W**
	Gamma_B25	7:0	Gamma_table B25 value.	
5Ch	**Gamma_B26**	**7:0**	**Default : 0d207**	**Access : R/W**
	Gamma_B26	7:0	Gamma_table B26 value.	
5Dh	**Gamma_B27**	**7:0**	**Default : 0d215**	**Access : R/W**
	Gamma_B27	7:0	Gamma_table B27 value.	
5Eh	**Gamma_B28**	**7:0**	**Default : 0d223**	**Access : R/W**
	Gamma_B28	7:0	Gamma_table B28 value.	
5Fh	**Gamma_B29**	**7:0**	**Default : 0d232**	**Access : R/W**
	Gamma_B29	7:0	Gamma_table B29 value.	
60h	**Gamma_B30**	**7:0**	**Default : 0d239**	**Access : R/W**
	Gamma_B30	7:0	Gamma_table B30 value.	
61h	**Gamma_B31**	**7:0**	**Default : 0d247**	**Access : R/W**
	Gamma_B31	7:0	Gamma_table B31 value.	
62h	**Gamma_B32**	**7:0**	**Default : 0d255**	**Access : R/W**
	Gamma_B32	7:0	Gamma_table B32 value.	

Scaler Register (Bank = 00, Registers B0h ~ FFh)

Scaler Register (Bank=00, Registers B0h ~ FFh)				
Index	**Mnemonic**	**Bits**	**Description**	
B0h	**LINE_SHIFT**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SEL_V_CLR	6	Select Vcounter Clear by DOWNCNT_EQ1 or EARLY_VS.	
	-	5	Reserved.	
	VCR_FF_MODE	4	Enable output VSYNC follow input VSYNC mode.	
	FIELD_INV_VS	3	Line shift vs Field Inverse.	
	LINE_SHIFT_NUM[2:0]	2:0	Line Shift Numbers.	

Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description	
B1h	**SYNC_CONTROL**	**7:0**	**Default : 0x08**	**Access : R/W**
	CLK_DLY[3:0]	7:4	Output clock delay select.	
	CLK_INV	3	Output Clock invert enable.	
	DE_INV	2	Output DE Invert enable.	
	VS_INV	1	Output VSYNC Invert enable.	
	HS_INV	0	Output HSYNC Invert enable.	
B2h	**SYNC_SEL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SEL_VDE	3	Select VDE output to VSYNC pin.	
	SEL_HDE	2	Select HDE output to HSYNC pin.	
	DATA_SKEW	1:0	Bus data Skew select.	
B3h ~ BFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
C0h	**HSPRDL_L**	**7:0**	**Default : -**	**Access : RO**
	HSPRDL[7:0]	7:0	Number of system clock count at 512 HSYNCs.	
C1h	**HSPRDL_M**	**7:0**	**Default : -**	**Access : RO**
	HSPRDL[15:8]	7:0	Number of system clock count at 512 HSYNCs.	
C2h	**HSPRDL_H**	**7:0**	**Default : -**	**Access : RO**
	HSPRDL[23:16]	7:0	Number of system clock count at 512 HSYNCs.	
C3h	**YCDLYCTL**	**7:0**	**Default : 0x00**	**Access : R/W**
	LNBF4_MD	7	Four Line Buffer Mode.	
	VSD_PIPE	6	VSD Pipe select. 0: Original. 1: Early pipe 2 cycle.	
	-	5:3	Reserved.	
	YC_DLY_CTL	2:0	YC Delay Control. 000: Normal. 001: Y early 1 cycle. 010: Y early 2 cycles. 011: Y early 3 cycles. 100: Normal. 101: C early 1 cycle. 110: C early 2 cycles. 111: C early 3 cycles.	
C4h	**VTOTAL_MAX_L**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TOTAL_MAX[7:0]	7:0	Vertical Max Total (lower 8 bits).	
C5h	**VTOTAL_MAX_H**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:3	Reserved.	
	TOTAL_MAX[10:8]	2:0	Vertical Max Total (higher 3 bits).	
C6h ~	**-**	**7:0**	**Default : -**	**Access : -**

Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description	
C7h	-	7:0	Reserved.	
C8h	**ATGCTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAXR (RO)	7	Max value flag for Red channel (read only). 0: Normal. 1: Max value (255) value when AGR = 0. Output over max value (255) when AGR = 1.	
	MAXG (RO)	6	Max value flag for Green channel (read only). 0: Normal. 1: Max value (255) value when AGR = 0. Output over max value (255) when AGR = 1.	
	MAXB (RO)	5	Max value flag for Blue channel (read only). 0: Normal. 1: Max value (255) value when AGR = 0. Output over max value (255) when AGR = 1.	
	AC_EN	4	ADC Calibration Enable. 0: Disable. 1: Enable.	
	AGR	3	Auto Gain Result selection. 0: Output has max/min value. 1: Output is overflow/underflow.	
	ATGM	2	Auto Gain Mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared till ATGE = 0).	
	ATGR (RO)	1	Auto Gain Result Ready. 0: Result not ready. 1: Result ready.	
	ATGE	0	Auto Gain Function Enable. 0: Disable. 1: Enable.	
C9h	**ATGST**	**7:0**	**Default : -**	**Access : R/W**
	VCLP	7	Video auto gain mode. 0: RGB mode. 1: YPbPr Mode.	
	-	6	Reserved.	
	CALR (RO)	5	Calibration value flag for Red channel. 0: Normal. 1: Calibration result (needs to increase offset) when ACE=1.	
	CALG (RO)	4	Calibration value flag for Green channel. 0: Normal. 1: Calibration result (needs to increase offset) when ACE=1.	
	CALB (RO)	3	Calibration value flag for Blue channel. 0: Normal. 1: Calibration result (needs to increase offset) when ACE=1.	

Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description	
	MINR (RO)	2	Min value flag for Red channel. 0: Normal. 1: Min value (0) present when AGR = 0, ACE = 0. Output under min value (0) when AGR = 1, ACE = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	MING (RO)	1	Min value flag for Green channel. 0: Normal. 1: Min value (0) present when AGR = 0, ACE = 0. Output under min value (0) when AGR = 1, ACE = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	MINB (RO)	0	Min value flag for Blue channel. 0: Normal. 1: Min value (0) present when AGR = 0, ACE = 0. Output under min value (0) when AGR = 1, ACE = 0. Calibration result (needs to decrease offset) when ACE = 1.	
CAh	**ATFCHSEL**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ATPCHSEL[1:0]	5:4	Auto Phase R/G/B channel select 00: R/G/B 3 channels 01: only R channel 10: only G channel 11: only B channel	
	-	3	Reserved.	
	ATGCHSEL[2:0]	2:0	Auto Gain R/G/B channel min/max value select. 000: R min value 001: G min value 010: B min value 011: R max value 100: G max value 101: B max value 11x: Reserved	
CBh	**ATOCTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	JITLR	7	Jitter function Left / Right result for 86h and 87h. 0: Left result. 1: right result.	
	JITS	6	Jitter Software clear. 0: Not clear. 1: Clear.	
	-	5	Reserved.	
	JITM	4	Jitter function Mode. 0: Update every frame. 1: Keep the history value.	
	JITR	3	Jitter function Result (Read Only). 0: No jitter. 1: Jitter present.	

Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description	
	ATOM	2	Auto position function Mode. 0: Update every frame. 1: Keep the history value.	
	ATOR	1	Auto position result Ready (Read Only). 0: Result ready. 1: Result not ready.	
	ATOE	0	Auto position function Enable. 0: Disable. 1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
CCh	**AOVDV**	**7:0**	**Default : 0x00**	**Access : R/W**
	AOVDV[3:0]	7:4	Auto position Valid Data Value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000. 0010: Valid if data >= 0010 0000. … … 1111: Valid if data >= 1111 0000.	
	-	3:0	Reserved.	
CDh	**ATGVALUE (RO)**	**7:0**	**Default: -**	**Access : RO**
	ATGVALUE[7:0]	7:0	Auto Gain result based on 7Ah[2:0].	
CEh	**AOVST-L (RO)**	**7:0**	**Default : -**	**Access : RO**
	AOVST [7:0]	7:0	Auto position detected result Vertical Starting point.	
CFh	**AOVST-H (RO)**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	AOVST[10:8]	2:0	See description for AOVST [7:0].	
D0h	**AOHST-L (RO)**	**7:0**	**Default : -**	**Access : RO**
	AOHST[7:0]	7:0	Auto position detected result Horizontal Starting point.	
D1h	**AOHST-H (RO)**	**7:0**	**Default : -**	**Access : DB**
	-	7:3	Reserved.	
	SPRGST[10:8]	2:0	Image horizontal sample start point, count by input dot clock.	
D2h	**AOVEND-L (RO)**	**7:0**	**Default : -**	**Access : RO**
	AOVEND[7:0]	7:0	Auto position detected result Vertical End point.	
D3h	**AOVEND-H (RO)**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	AOVEND[10:8]	2:0	See description for AOVEND[7:0].	
D4h	**AOHEND-L (RO)**	**7:0**	**Default : -**	**Access : RO**
	AOHEND[7:0]	7:0	Auto position detected result Horizontal End point.	
D5h	**AOHEND-H (RO)**	**7:0**	**Default : -**	**Access : RO**
	-	7:4	Reserved.	
	AOHEND[11:8]	2:0	See description for AOHEND[7:0].	

Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description	
D6h	**JLR-L (RO)**	**7:0**	**Default : -**	**Access : RO**
	JLR[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on Reg_7Bh[7].	
D7h	**JLR-H (RO)**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	JLR[10:8]	2:0	See description for JLR[7:0].	
D8h	**ANRF**	**7:0**	**Default : -**	**Access : RO**
	-	7:6	Reserved.	
	HNEN	5	High level Noise reduction Enable. 0: Disable. 1: Enable.	
	BGEN	4	Background Noise reduction Enable. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	ANLV[2:0]	2:0	Auto Noise Level, 000: Noise level = 1, 001: Noise level = 2, 010: Noise level = 4, 011: Noise level = 8, 100: Noise level = 9, 101: Noise level = 10, 110: Noise level = 12, 111: Noise level = 16.	
D9h	**ATPGTH**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATPGTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATPV3 when ATPN4 = 0.	
DAh	**ATPTTH**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATPTTH[7:0]	7:0	Auto Phase Text Threshold for ATPV4.	
DBh	**ATPCTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP_FLTRMD	7	0: Disable auto-position filter mode. 1: Enable auto-position filter mode.	
	GRY (RO)	6	Gray scale detect (read only).	
	TXT (RO)	5	Text detect (read only).	
	APMASK[2:0]	4:2	Nose Mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bit. 011: Mask 3 bit. 100: Mask 4 bit. 101: Mask 5 bit. 110: Mask 6 bit. 111: Mask 7 bit.	

Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description	
	ATPR (RO)	1	Auto Phase Result ready. 0: Result not ready. 1: Result ready.	
	ATPE	0	Auto Phase function Enable. 0: Disable. 1: Enable.	
DCh	**ATPV1 (RO)**	**7:0**	**Default : -**	**Access : RO**
	ATPVALUE[7:0]	7:0	Auto Phase Value.	
DDh	**ATPV2 (RO)**	**7:0**	**Default : -**	**Access : RO**
	ATPVALUE[15:8]	7:0	See description for ATPVALUE[7:0].	
DEh	**ATPV3 (RO)**	**7:0**	**Default : -**	**Access : RO**
	ATPVALUE[23:16]	7:0	See description for ATPVALUE[7:0].	
DFh	**ATPV4 (RO)**	**7:0**	**Default : -**	**Access : RO**
	ATPVALUE[31:24]	7:0	See description for ATPVALUE[7:0].	
E0h	**PDMD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCLK[1:0]	7:6	Gated Clock for SRAM. 00: Normal. 01: V Blank. 10: H Blank and V Blank. 11: Reserved.	
	AUXCLK_GAT	5	0: Enable MVD MCU-support Clock. 1: Disable MVD MCU-support Clock.	
	CMBCLK_GAT	4	0: Enable MVD comb-filter Clock. 1: Disable MVD comb-filter Clock.	
	-	3	Reserved.	
	EOCLK_INV	2	External OSD sample Clock Inverting.	
	IDCLK_INV	1	Scaler input sample Clock Inverting.	
	FSCCLK_INV	0	Sub-carrier Clock Inverting.	
E1h	**PDMD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDALL	7	All chip power down.	
	BIUCLK_GAT	6	0: Enable register interface clock. 1: Disable register interface clock.	
	OSDCLK_GAT	5	0: Enable OSD clock. 1: Disable OSD clock.	
	PCCLK_GAT	4	0: Enable CRT output suppot clock. 1: Disable CRT output suppot clock.	
	ADCCLK_GAT	3	0: Enable 3-channel ADC digital clock. 1: Disable 3-channel ADC digital clock.	
	VDCLK_GAT	2	0: Enable CCIR and MVD interface clock. 1: Disable CCIR and MVD interface clock.	
	IDCLK_GAT	1	0: Enable scaler clock. 1: Disable scaler clock.	

Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description	
	FSCCLK_GAT	0	0: Enable MVD digital front-end clock. 1: Disable MVD digital front-end clock.	
E2h	**SWRST0**	**7:0**	**Default : 0x00**	**Access : R/W**
	REGR	7	Register Reset. 0: Normal operation. 1: Reset Register.	
	ADCR	6	ADC Reset. 0: Normal operation. 1: Reset ADC.	
	IPR	5	Digital Input Port Reset. 0: Normal operation. 1: Reset.	
	OP1R	4	Scaler Reset. 0: Normal operation. 1: Reset.	
	OP2R	3	Display Port Reset. 0: Normal operation. 1: Reset.	
	-	2	Reserved.	
	OSDR	1	Internal OSD Reset. 0: Normal operation. 1: Reset internal OSD.	
	SWR	0	Software Reset (reset All digital core except system registers). 0: Normal operation. 1: Reset.	
E3h	**SWRST1**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFER	7	Video Decoder Front End Reset. 0: Normal operation. 1: Reset.	
	VCFR	6	Video Decoder Comb Filter Reset. 0: Normal operation. 1: Reset.	
	MCUR	5	Embedded MCU Reset. 0: Normal operation. 1: Reset.	
	MCUR	4	GMC digital tune Reset. 0: Normal operation. 1: Reset.	
	-	3:0	Reserved.	
E4h	**ISOVRD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SL	7	Shift Line. 0: Shift line method 0. 1: Shift line method 1 for interlace mode.	
	CSHS	6	HSYNC in coast. 0: HSYOUT (recommended). 1: Re-shaped HSYNC.	

Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description	
	UVSP	5	User defined input VSYNC Polarity, active when IVSJ =1. 0: Active low. 1: Active high.	
	IVSJ	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (UVSP).	
	UHSP	3	User defined input HSYNC Polarity, active when IVSJ =1. 0: Active low. 1: Active high.	
	IHSJ	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (UHSP).	
	UINT	1	User defined non-interlace/interlace, active when INTJ = 1. 0: Non-interlace. 1: Interlace.	
	INTJ	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (UINT).	
E5h	**MDCTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_TEST_MD	7:6	IP Test-bus selection.	
	VERR	5	Video CCIR656 Error correct. 0: Disable. 1: Enable.	
	Field_ABSMD	4	Field Postion Absolute Value Mode.	
	VFIV	3	Video Field Inversion. 0: Normal. 1: Invert.	
	VEXF	2	Video External Field. 0: Use result of internal circuit detection. 1: Use external field.	
	INTF	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.	
	IFI	0	Interlace Field Inverting. 0: Normal. 1: Invert.	
E6h	**HSPW (RO)**	**7:0**	**Default : -**	**Access : RO**
	HS_PW	7:0	HS Pulse Width	
E7h	**VFREE**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTOOPCOAST_CLR	7	Set Auto-Coast-for-output status.	
	AUTOOPCOAST	6	Enable Auto-Coast-for-output.	
	MIN_VTT[5:0]	5:0	Minimum VTT to free-run.	
E8h	**HSTOL**	**7:0**	**Default : 0x05**	**Access : R/W**
	VS2HS (RO)	7	Input VSYNC too close to input HSYNC.	

Scaler Register (Bank=00, Registers B0h ~ FFh)

Index	Mnemonic	Bits	Description	
	LN4_DETMD	6	4 Line Detect Mode for Hs, DE.	
	HSTOL[5:0]	5:0	HSYNC Tolerance. 5: Default value.	
E9h	**VSTOL**	**7:0**	**Default : 0x01**	**Access : R/W**
	AUTONOSIGNAL_CLR	7	Set Auto-No-Signal status.	
	AUTONOSIGNAL	6	Enable Auto-No-Signal function.	
	HTT_FILTERMD	5	HTT Filter Mode.	
	HVTT_LOSE_MD	4	HVTT Lose Mode. 0: Original. 1: New by WDT sample.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance. 1: Default value.	
EAh	**HSPRD_L**	**7:0**	**Default : -**	**Access : RO**
	HSPRD[7:0]	7:0	Input Horizontal Period, count by reference clock.	
EBh	**HSPRD_H**	**7:0**	**Default : -**	**Access : RO**
	-	7:5	Reserved.	
	HSPRD[12:8]	4:0	See description for HSPRD[7:0].	
ECh	**VTOTAL_L**	**7:0**	**Default : -**	**Access : RO**
	VTOTAL[7:0]	7:0	Input Vertical Total Length, count by HSYNC.	
EDh	**VTOTAL_H**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	VTOTAL[10:8]	2:0	See description for VTOTAL[7:0].	
EEh	**PDMD2**	**7:0**	**Default : 0x60**	**Access : RW**
	MCUCLK_SEL	7	MCU Clock Source Select. 0: XTAL. 1: MPLL divided.	
	MCUDIV	6:4	MCU Clock divided by MPLL. 000: 4. 001: 6. 010: 8. 011: 10. 100: 12. 101: 14. 110: 16.	
	-	3:1	Reserved.	
	CC_GAT	0	Comb Clock Gating. 1: Gating mode. 0: No gating.	
EFh	**STATUS2 (RO)**	**7:0**	**Default : -**	**Access : RO**
	HTT_CHG_CS	7	Htotal change in CSOG.	
	-	6	Reserved.	

Scaler Register (Bank=00, Registers B0h ~ FFh)				
Index	**Mnemonic**	**Bits**	**Description**	
	STD_PAL	5	0: NTSC. 1: PAL.	
	CSD	4	CSYNC Detected status. 0: Input is not CSYNC. 1: Input is detected as CSYNC.	
	INTM	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.	
	INTF	2	Input odd/even Field detecting result by this chip. 0: Even. 1: Odd.	
	IHSP	1	Incoming input HSYNC Polarity detecting result by this chip. 0: Active low. 1: Active high.	
	IVSP	0	Incoming input VSYNC Polarity detecting result by this chip. 0: Active low. 1: Active high.	
F0h	**CHIP_ID**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_ID[7:0]	7:0	Chip id is 70h	
F1h	**CHIP_VERSION**	**7:0**	**Default : 0x01**	**Access : RO**
	CHIP_VER[7:0]	7:0	Version is 01h	
F2h ~ F3h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
F4h	**TRISTATE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OBBUS_TRI	4	Output bus Tristate.	
	VS_TRI	3	Output VSYNC Tristate.	
	HSY_TRI	2	Output HSYNC Tristate.	
	DE_TRI	1	Output DE Tristate.	
	CLK_TRI	0	Output CLK Tristate.	
F7h ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

Analog Register (Bank = 01)

Analog Register (Bank = 01)				
Index	**Name**	**Bits**	**Description**	
01h	**DBFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DBVB	0	Double Buffer load at Vertical Blanking. 0: Disable. 1: Enable.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
02h	**PLLDIVM**	**7:0**	**Default : 0x69**	**Access : R/W**
	PLLDIV[11:4]	7:0	PLL Divider ratio. ADC PLL will multiply the horizontal line frequency by PLLDIV[11:0]+3 to generate the ADC sampling clock.	
03h	**PLLDIVL**	**7:0**	**Default : 0x50**	**Access : R/W**
	PLLDIV[3:0]	7:4	PLL Divider ratio. ADC PLL will multiply the horizontal line frequency by PLLDIV[11:0]+3 to generate the ACD sampling clock. PLLDIV[11:0] default value: 1685 (1688-3).	
		3:0	Reserved.	
04h	**RGAIN_ADC**	**7:0**	**Default : 0x80**	**Access : R/W**
	RGAIN_ADC[7:0]	7:0	ADC Red channel Gain adjust.	
05h	**GGAIN_ADC**	**7:0**	**Default : 0x80**	**Access : R/W**
	GGAIN_ADC[7:0]	7:0	ADC Green channel Gain adjust.	
06h	**BGAIN_ADC**	**7:0**	**Default : 0x80**	**Access : R/W**
	BGAIN_ADC[7:0]	7:0	ADC Blue channel Gain adjust.	
07h	**ROFFS_ADC**	**7:0**	**Default : 0x80**	**Access : R/W**
	ROFFS_ADC[7:0]	7:0	ADC Red channel Offset adjust.	
08h	**GOFFS_ADC**	**7:0**	**Default : 0x80**	**Access : R/W**
	GOFFS_ADC[7:0]	7:0	ADC Green channel Offset adjust.	
09h	**BOFFS_ADC**	**7:0**	**Default : 0x80**	**Access : R/W**
	BOFFS_ADC[7:0]	7:0	ADC Blue channel Offset adjust.	
0Ah	**CLPACE**	**7:0**	**Default : 0x05**	**Access : R/W**
	CLPACE	7:0	Clamp Placement based on ADC clock.	
0Bh	**CLDUR**	**7:0**	**Default : 0x05**	**Access : R/W**
	CLDUR	7:0	Clamp Duration based on ADC clock.	
0Ch	**GCTRL**	**7:0**	**Default : 0x82**	**Access : R/W**
	HSP	7	Input HSYNC Polarity. 0: Active low. 1: Active high.	
	ECLK	6	External Clock. 0: ADC clock from internal ADC PLL. 1: ADC clock from external clock.	
	HSLE	5	HS Lock Edge. Determines which edge of HSYNC the ADC PLL will lock to, assuming HSP is set correctly. 0: Leading edge of HSYNC. 1: Trailing edge of HSYNC.	
	CLPE	4	Clamp reference Edge. 0: Trailing edge of HSYNC. 1: Leading edge of HSYNC.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	CCDIS	3	Disable PLL watchdog timer. 0: Always enable clamp. 1: Disable clamp during active coast.	
	WDIS	2	Disable watchdog timer. 0: Enable PLL watchdog timer. A watchdog timer is used to reset the ADC PLL when the PLL remains much higher than PLLDIV*HSYNC_FREQ for a predetermined period. See WDTOL (Register 30h). 1: Disable PLL watchdog timer (should only be used when DPL_S=0).	
	CSTP	1	Coast Polarity. 0: Active low. 1: Active high.	
	-	0	Reserved.	
0Dh	**BWCOEF**	**7:0**	**Default : 0x85**	**Access : R/W**
	BWCOEF[7:6]	7:6	Damping coefficient mode control. 00: Default value – backward compatibility mode. 01: Reserved. 10: Automatic DCOEF control (recommended mode). 11: Reserved.	
	BWCOEF[5:0]	5:0	PLL loop filter control.	
0Eh	**FCOEF**	**7:0**	**Default : 0x09**	**Access : R/W**
	-	7:5	Reserved.	
	FREQCOEF[4:0]	4:0	PLL loop filter control.	
0Fh	**DCOEF**	**7:0**	**Default : 0x03**	**Access : R/W**
		7:4	Reserved.	
	DAMPCOEF[3:0]	3:0	PLL loop filter control.	
10h	**CLKCTRL1**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7	Reserved.	
	STAT[2]	6	Status select; selects internal PLL status values to read from register 1Eh.	
	PHASEADC	5:0	Clock Phase adjust for ADC (set to PHASECC+8).	
11h	**CLKCTRL2**	**7:0**	**Default : 0x00**	**Access : R/W**
	STAT[1:0]	7:6	Status select; selects 1/8 internal PLL status values to read from register 1Eh.	
	PHASECC[5:0]	5:0	Clock phase adjust for ADC sampling time point; phase is adjustable between 0 and 360° in 5.6° steps.	
12h	**VCOCTRL**	**7:0**	**Default : 0x15**	**Access : R/W**
	PDGT	7	Phase digitizer frequency compensation disable.	
	-	6:4	Reserved.	
	SETCNT[3:0]	3:0	Setting time for ADC PLL phase detector, in ADC clock periods.	
13h	**RT_CT**	**7:0**	**Default : 0xC6**	**Access : R/W**

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	TOLCN[1:0]	7:6	Watchdog maximum Count. 0: 0. 1: 4. 2: 32. 3: 127.	
	IQ1LEN[2:0]	5:3	Counter for IQ from high to low.	
	IQ0LEN[2:0]	2:0	Counter for IQ from low to high.	
14h	**SOG_LVL**	**7:0**	**Default : 0x10**	**Access : R/W**
	RMID	7	Middle clamp of Red Channel. 0: Disable. 1: Enable (used when YPbPr input).	
	BMID	6	Middle clamp of Blue Channel. 0: Disable. 1: Enable (used when YPbPr input).	
	-	5:0	Reserved.	
15h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
16h	**DITHCTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIT_TOG_LEN4	7	0: Select Length 2 Toggle Loop. 1: Select Length 4 Toggle Loop.	
	DIT_TOG_R	6	1: Enable ADC R Toggle Dither.	
	DIT_TOG_G	5	1: Enable ADC G Toggle Dither.	
	DIT_TOG_B	4	1: Enable ADC B Toggle Dither.	
	DIT_LVL_CAL	3:2	Select ADC Dither Level for CAL.	
	DIT_LVL	1:0	Select ADC Dither Level for display.	
17h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
18h	**CALEN**	**7:0**	**Default : 0x00**	**Access : R/W**
	CALG_EN	7	ADC gain auto-cal function enable. 0: Disable. 1: Enable.	
	CALG_UPD	6	Auto update GAIN enable. 0: Disable. 1: Enable.	
	TRIG_CALG	5	Trigger gain calibration enable. 0: Disable. 1: Enable.	
	CALO_EN	4	ADC offset auto-cal function enable. 0: Disable. 1: Enable.	
	CALO_UPD	3	Auto update offset enable. 0: Disable. 1: Enable.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	TRIG_CALO	2	Trigger offset calibration enable. 0: Disable. 1: Enable.	
	CAL_CHAN	1:0	Select manual mode calibration channel. 00: R. 01: G. 10: B. 11: Reserved.	
19h	**CALCTL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CAL_UPD_HS	5	Update CAL value during HS. 0: Disable. 1: Enable.	
	CAL_ONESHOTZ	4	CAL on one-shot loop/real time. 0: CAL on one-shot loop time. 1: CAL on one-shot real time.	
	CAL_STOP	3	Stop (halt) auto offset calibration. 0: Disable. 1: Enable.	
	CAL_MODE2	2	Auto-stop calibration after 128 frames. 0: Enable. 1: Disable.	
	BYPASSDOUT	1	Bypass DOUT during CAL. 0: Disable. 1: Enable.	
	CAL_EDGE	0	CAL from HS leading/trailing edge. 0: CAL from HS leading edge. 1: CAL from HS trailing edge.	
1Ah	**CALSMP**	**7:0**	**Default : 0x00**	**Access : R/W**
	STATUS_SEL[2:0]	7:5	Select status of STATUS_CAL. 000: {CAL_DOUT[5:0], 1'b0, CAL_DONE}. 001: Calibrated R offset. 010: Calibrated G offset. 011: Calibrated B offset. 100: CAL_DOUT[13:6]. 101: Digital Offset R. 110: Digital Offset G. 111: Digital Offset B.	
	SMPDLY_EN	4	Use default/SMPDLY as CAL sample delay. 0: Use internal default as CAL sample delay. 1: Use SMPDLY as CAL sample delay.	
	SMPDLY	3:0	Calibration sample delay.	
1Bh	**CALDUR**	**7:0**	**Default : 0x00**	**Access : R/W**
	CALCNT_EN	7	Use default/CALDLY-CALDUR to generate CAL pulse. 0: Use default to generate CAL pulse. 1: Use CALDLY-CALDUR to generate CAL pulse.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	CALDUR[6:0]	6:0	CAL pulse duration register.	
1Ch	**CALDLY**	**7:0**	**Default : 0x00**	**Access : R/W**
	CALDLY[7:0]	7:0	CAL pulse delay register.	
1Dh	**STATUS_CAL**	**7:0**	**Default : -**	**Access : RO**
	Note: Calibration status is read based on STATUS_SEL[2:0] (Bank 01, Reg_1Ah[7:5]).			
	STATUS_SEL[2:0]			
	7:5 4 3 2 1 0		Reserved. CAL_DOUT[13:6]. CAL_OFFSB. CAL_OFFSG. CAL_OFFSR. {CAL_DOUT[5:0], 1'b0, CAL_DONE}.	
1Eh	**STATUS_PLL**	**7:0**	**Default : -**	**Access : RO**
	Note: PLL status is read based on STAT[2:0] (Bank 01, Reg_10h[6] and Bank 02, Reg-11h[76]).			
	STAT[2:0]			
	000	7 6 5 4 3 2 1 0	[2'd0, SAR_MIN]. {2'd0, SAR_MAX}. {SAR_AVG[19:12]. {1'b0, ICAl_s[6:0]}. {1'b0, SAR_s[6:0]}. {FREQCTRL[15:8]}. {FREQCTRL[23:16]}. {LOCK, IQ, SLOW, FAST, FREERUN, 3'b000}.	
1Fh ~ 22h	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
23h	**FPLL_STATUS**	**7:0**	**Default : -**	**Access : RO**
	FPLL_STATUS[7:0]	7:0	FPLL Status.	
24h		**7:0**	**Default : 0x40**	**Access : R/W**
	-	7:5	Reserved.	
	FPLL_MD	4	FPLL Mode selection. 0: CVBS. 1: RGB.	
	-	3:0	Reserved.	
25h	**FPLL_DIVN**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FPLL_DIVN[3:0]	3:0	FPLL Feed back Divider. 0000: Divide by 1. 0001: Divide by 2. 0010: Divide by 3. … 1111: Divide by 16.	
26h ~ 28h	-	**7:0**	**Default : -**	**Access : -**
	-	7:5	Reserved.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
29h	**ADC_REG**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ADC_IMD	4:3	Set ADC total current.	
	RENC_ADC	2	RGB mode: set to 0/CVBS mode: set to 1.	
	GENC_ADC	1	RGB mode: set to 0/CVBS mode: set to 1.	
	BENC_ADC	0	RGB mode: set to 0/CVBS mode: set to 1.	
2Ah ~ 2Bh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
2Ch	**RGB_BW_SEL1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	-	5:4	Reserved.	
	-	3	Reserved.	
	R_BW[2:0]	2:0	R-channel input filter BW select. 000: 200 MHz. 001: 165 MHz. 010: 130 MHz. 011: 87 MHz. 100: 65 MHz. 101: 30 MHz. 110: 10 MHz. 111: 6 MHz.	
2Dh	**RGB_BW_SEL2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	G_BW[2:0]	6:4	G-channel input filter BW select.	
	-	3	Reserved.	
	B_BW[2:0]	2:0	B-channel input filter BW select.	
2Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
2Fh	**ADC_MUX**	**7:0**	**Default :**	**Access :**
	-	7:6	Reserved.	
	MUX[5:0]	5:0	See ADC MUX TABLE.	
30h ~ 8Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
90h	**SARADC_CTRL**	**7:0**	**Default : 0x40**	**Access : R/W**
	SAR_SNGL_CHNL	1:0	Channel selection in Single Channel mode.	
	-	3:2	Reserved.	
	SAR_SNGL	4	Single channel mode enable. Only sample channel at bit[1:0]	
	SAR_FREERUN	5	SARADC sample mode. 1: Freerun mode. 0: One shot mode.	
	-	6	Reserved.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	SAR_START	7/W	SARADC sample Start.	
	SAR_RDY	7/R	SARADC sample Ready.	
91h	**SARADC_SAMPRD**	**7:0**	**Default : 0x20**	**Access : R/W**
	CKSAMP_PRD	7:0	SARADC input Sample Period in one shot mode. Real_SAMP_PRD = CKSAMP_PR x 4	
92h	**SARADC_AISEL**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_AISEL	3:0	SAR_AISEL[3:0]: Input select of PAD_SAR_GPIO SAR_AISEL[i]=1b'0: Digital GPIO Input SAR_AISEL[i]=1b'1: SAR ADC Analog Input	
	-	7:4	Reserved	
93h	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
94h	**SAR_CH1_UPB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	REG_SAR_CH1_UPB [5:0]	5:0	The voltage Upper Bound in MCU sleep mode for Channel 1 keypad wake up.	
95h	**SAR_CH1_LOB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	REG_SAR_CH1_LOB [5:0]	5:0	The voltage Lower Bound in MCU sleep mode for Channel 1 keypad wake up.	
96h	**SAR_CH2_UPB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved	
	REG_SAR_CH2_UPB [5:0]	5:0	The voltage Upper Bound in MCU sleep mode for Channel 2 keypad wake up.	
97h	**SAR_CH2_LOB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved	
	REG_SAR_CH2_LOB [5:0]	5:0	The voltage Lower Bound in MCU sleep mode for Channel 2 keypad wake up.	
98h	**SAR_CH3_UPB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved	
	REG_SAR_CH3_UPB [5:0]	5:0	The voltage Upper Bound in MCU sleep mode for Channel 3 keypad wake up.	
99h	**SAR_CH3_LOB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	REG_SAR_CH3_LOB [5:0]	5:0	The voltage Lower Bound in MCU sleep mode for Channel 3 keypad wake up.	
9Ah ~ 9Bh	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
9Ch	**ADC_MD_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADC_DCTRL	7:6	Reserved for ADC DCTRL.	
	GSHIFT_R	5	1: Enable ADC R Gain Range Shift for VD Mode.	
	GSHIFT_G	4	1: Enable ADC G Gain Range Shift for VD Mode.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	GSHIFT_B	3	1: Enable ADC B Gain Range Shift for VD Mode.	
	ADC_VCTRL	2:0	ADC Voltage Control (Recommend Setting = 3'b011).	
9Dh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
9Eh	**CAL_CTRL3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CAL_STSWEN	6	1: Enable Write to Internal CAL Registers through STATUS_CAL.	
	CAL_SWOV	5:4	00: Normal Mode. 01: Switch ADC Input to Offset CAL Reference Voltage. 10: Reserved. 11: Reserved.	
	CAL_HOLD	3	1: Hold Current CAL Result for Display.	
	CAL_INPUT	2	0: CAL to Internal Offset Reference Voltage. 1: CAL to ADC Input.	
	CAL_HYS	1	1: Enable CAL Update Hytheresis.	
	DOFFS_EN	0	1: Enable Digital Offset Adjustment.	
9Fh	**ADCTOUT**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ADCTOUT_SYNC	3	1: Enable ADC Test Out Sync to CKEXT.	
	ADCTOUT_DIV	2:0	Select ADC Test Out Decimation Ratio (1~8).	
A0h	**RG_DRV**	**7:0**	**Default : 0x55**	**Access : R/W**
	G[7:6]_DRV[1:0]	7:6	Pad G[7:4] Driving select.	
	G[5:4]_DRV[1:0]	5:4	Pad G[3:0] Driving select.	
	R[3:2]_DRV[1:0]	3:2	Pad R[7:4] Driving select.	
	R[1:0]_DRV[1:0]	1:0	Pad R[3:0] Driving select.	
A1h	**RG_DRV**	**7:0**	**Default : 0x55**	**Access : R/W**
	HS_DRV[1:0]	7:6	Pad Hsync Driving select.	
	VS_DRV[1:0]	5:4	Pad Vsync Driving select.	
	B[7:4]_DRV[1:0]	3:2	Pad B[7:4] Driving select.	
	B[3:0]_DRV[1:0]	1:0	Pad B[3:0] Driving select.	
A2h	**RG_DRV**	**7:0**	**Default : 0x55**	**Access : R/W**
	PWM2_DRV[1:0]	7:6	Pad PWM2 Driving select.	
	PWM1_DRV[1:0]	5:4	Pad PWM1 Driving select.	
	CLK_DRV[1:0]	3:2	Pad CLK Driving select.	
	DE_DRV[1:0]	1:0	Pad DE Driving select.	
A3h	**EPD_R**	**7:0**	**Default : 0x00**	**Access : R/W**
	EPD_R[7:0]	7:0	Enable Pull Down in R channel.	
A4h	**EPD_G**	**7:0**	**Default : 0x00**	**Access : R/W**
	EPD_G[7:0]	7:0	Enable Pull Down in G channel.	
A5h	**EPD_B**	**7:0**	**Default : 0x00**	**Access : R/W**

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	EPD_B[7:0]	7:0	Enable Pull Down in B channel.	
A6h	**EPD_R**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	EPD_PWM2	5	Enable pull down in PWM2 pad.	
	EPD_PWM1	4	Enable pull down in PWM2 pad.	
	EPD_CLK	3	Enable pull down in CLK pad.	
	EPD_DE	2	Enable pull down in DE pad.	
	EPD_HS	1	Enable pull down in HSYNC pad.	
	EPD_VS	0	Enable pull down in VSYNC pad.	
A7h ~ AAh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
ABh	**VDAC_ADJ2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ED[4:0]	4:0	Testing control for voltage DAC.	
ACh ~ C9h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
CAh	**POL_SET0**	**7:0**	**Default : 0x00**	**Access : R/W**
	POL_OUT_INV	7	POL Output Invert.	
	POL_TP	6:0	POL Transition Point.	
CBh	**POL_SET1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	POL_SEL	4	0: VSYNC Frequency POL. 1: HSYNC Frequency POL.	
	POL_PVI_10IN	3	POL Output to SEQ_MOD Pin if EFh[7] = 0.	
	-	2:0	Reserved.	
CCh	**SCAL_ACT**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	TC_CLK_DIV2	5	TC Clock Divide 2.	
	-	4	Reserved.	
	LINE_ACT_D1L	3	Line Active Delay One Line time.	
	LINE_ACT_EN	2	TCON Line_Extract Mode work with Digital V_Scaling.	
	-	1:0	Reserved.	
CDh	**GPO_OEV2_WIDTH**	**7:0**	**Default : 0x54**	**Access : R/W**
	GPO_OEV2_DIS	7	OEV2 Disable.	
	GPO_OEV2_WIDTH [6:0]	6:0	OEV2 Pulse Width.	
CEh	**GPO_OEV3_WIDTH**	**7:0**	**Default : 0x54**	**Access : R/W**
	GPO_OEV3_DIS	7	OEV3 Disable.	
	GPO_OEV3_WIDTH [6:0]	6:0	OEV3 Pulse Width.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
CFh	**GPO_OEV_ DELTA**	**7:0**	**Default : 0x54**	**Access : R/W**
	-	7:4	Reserved.	
	GPO_OEV_ DELTA[3:0]	3:0	Adjust OEV distance.	
D0h	**PTC_MODE1**	**7:0**	**Default : 0x8C**	**Access : R/W**
	TC_MD	7	TC signal output enable. 0: Disable set low. 1: Enable.	
	OEV_DELTA_EN	6	OEV distance adjust Enable.	
	DOU_EXTR_MD[1:0]	5:4	00: Normal mode. 01: Paranoma extract mode. 10: Full extract mode. 11: Line duplicate mode.	
	FRAME_INV_EN	3	0: Disable. 1: Enable.	
	EARLY_VS	2	Early vs.	
	FIELD_SEL	1	Select field inverse from IP.	
	LN_SHIFT	0	Field Line Shift enable.	
D1h	**PTC_MODE2**	**7:0**	**Default : 0x3E**	**Access : R/W**
	TCCLK_CONF[1:0]	7:6	7: 13 CLK swap. 6: 3 CLK inverse.	
	SEQ_MD	5	0: Single clock output mode. 1: Three clock output mode.	
	TCCLK_MD	4	Select 3TC CLK or 1 TC CLK.	
	STHLR_SEL	3	0: STHR. 1: STHL.	
	STVLR_SEL	2	0: STVR. 1: STVL.	
	L_R	1	0: L_R equal 0. 1: L_R equal 1.	
	U_D	0	0: U_D=0. 1: U_D=1.	
D2h	**PTC_MODE3**	**7:0**	**Default : 0x84**	**Access : R/W**
	SET_TCCLK23_VALUE	7	Set TCCLK23 High/Low.	
	LG_MD	6	LG_panel Mode enable.	
	DF_EXT_LN	5	Different frame, Different Extract Line mode. 0: Disable. 1: Enable.	
	LN_DUP_MD[1:0]	4:3	Duplicate 2/3 Line Mode. 4: OEV3 enable. 3: OEV2 enable.	
	FIELD_IN_SEL	2	Select Field source from OP2 or free-run.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	LINE_INV_DIS	1	Line Inverse Disable. 0: Enable. 1: Disable.	
	FRP_VCOM_INV	0	VCOM Inverse to FRP.	
D3h	**LN_EXTR_CNT_LMT**	**7:0**	**Default : 0xDD**	**Access : R/W**
	LN_EXTR_CNT_LMT2	7:4	Line Extract/duplicate Counter 2.	
	LN_EXTR_CNT_LMT1	3:0	Line Extract/duplicate Counter 1.	
D4h	**LN_EXTR_SET1_H**	**7:0**	**Default : 0x2F**	**Access : R/W**
	LN_EXTR_SET1[7:0]	7:0	Line Extract/duplicate set 1 High byte.	
D5h	**LN_EXTR_SET1_L**	**7:0**	**Default : 0xEF**	**Access : R/W**
	LN_EXTR_SET1[15:8]	7:0	Line Extract/duplicate set 1 Low byte.	
D6h	**LN_EXTR_SET2_H**	**7:0**	**Default : 0x1F**	**Access : R/W**
	LN_EXTR_SET2[7:0]	7:0	Line Extract/duplicate set 2 High byte.	
D7h	**LN_EXTR_SET2_L**	**7:0**	**Default : 0xE7**	**Access : R/W**
	LN_EXTR_SET2[15:8]	7:0	Line Extract/duplicate set 2 Low byte.	
D8h	**EXTR_STT_LN1**	**7:0**	**Default : 0x02**	**Access : R/W**
	EXTR_STT_LN1[7:0]	7:0	Line Extract/duplicate Start Line 1.	
D9h	**EXTR_END_LN1**	**7:0**	**Default : 0x30**	**Access : R/W**
	EXTR_END_LN1[7:0]	7:0	Line Extract/duplicate End Line 1.	
DAh	**EXTR_STT_LN2**	**7:0**	**Default : 0x50**	**Access : R/W**
	EXTR_STT_LN2[7:0]	7:0	Line Extract/duplicate Start Line 2.	
DBh	**EXTR_END_LN2**	**7:0**	**Default : 0x77**	**Access : R/W**
	EXTR_END_LN2[7:0]	7:0	Line Extract/duplicate End Line 2.	
DCh	**GPO_FRP_TRAN**	**7:0**	**Default : 0x13**	**Access : R/W**
	OUT_INV	7	Output Inverse.	
	GPO_FRP_TRAN_MULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_FRP_TRAN[4:0]	4:0	FRP Transition position.	
DDh	**GPO_STH_STT**	**7:0**	**Default : 0x46**	**Access : R/W**
	OUT_INV	7	Output Inverse.	
	GPO_STH_STT_MULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_STH_STT[4:0]	4:0	STH pulse Start position.	
DEh	**GPO_STH_WIDTH**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:6	Reserved.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	GPO_STH_WIDTH_ MULT[1:0]	5:4	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_STH_WIDTH [3:0]	3:0	STH pulse Width.	
DFh	**GPO_OEH_STT**	**7:0**	**Default : 0xA3**	**Access : R/W**
	OUT_INV	7	Output Inverse.	
	GPO_OEH_STT_MULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_OEH_ STT[4:0]	4:0	OEH pulse Start position.	
E0h	**GPO_OEH_WIDTH**	**7:0**	**Default : 0x0B**	**Access : R/W**
	-	7:6	Reserved.	
	GPO_OEH_WIDTH_ MULT[1:0]	5:4	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_OEH_WIDTH [3:0]	3:0	OEH pulse Width.	
E1h	**GPO_ OEV _STT**	**7:0**	**Default : 0x01**	**Access : R/W**
	OUT_INV	7	Output Inverse.	
	GPO_OEV_STT_MMU LT[1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_OEV_STT[1:0]	4:0	OEV pulse Start.	
E2h	**GPO_OEV_WIDTH**	**7:0**	**Default : 0x6D**	**Access : R/W**
	-	7:6	Reserved.	
	GPO_OEV_WIDTH_ MULT[1:0]	5:4	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_OEV_WIDTH [3:0]	3:0	OEV pulse Width.	
E3h	**GPO_CKV_STT**	**7:0**	**Default : 0x2D**	**Access : R/W**
	OUT_INV	7	Output Inverse.	
	CKV_STT_ MULT[1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_ CKV_STT[4:0]	4:0	CKV pulse Start.	
E4h	**GPO_CKV_STT2**	**7:0**	**Default : 0x04**	**Access : R/W**

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	-	7:6	Reserved.	
	CKV_STT2_MULT [1:0]	5:4	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_ CKV_ST2[3:0]	3:0	CKV pulse Start 2.	
E5h	**GPO_CKV_WIDTH**	**7:0**	**Default : 0x5F**	**Access : R/W**
	-	7	Reserved.	
	CKV_WIDTH_ MULT[1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_ CKV_WIDTH[4:0]	4:0	CKV pulse width.	
E6h	**GPO_STV_LN_TH**	**7:0**	**Default : 0x46**	**Access : R/W**
	-	7	Reserved.	
	GPO_STV_1LN	6	STV width is 1 Line.	
	GPO_ STV _LINE_TH	5:0	STV line position	
E7h	**GPO_ STV _STT**	**7:0**	**Default : 0x29**	**Access : R/W**
	OUT_INV	7	Output Inverse.	
	STV_STT_MULT[1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_ STV_STT[4:0]	4:0	STV pulse Start.	
E8h	**GPO_STV_ WIDTH**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	STV_WIDTH_MULT [1:0]	5:4	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_STV_WIDTH [3:0]	3:0	STV pulse Width.	
E9h	**GPO_OEV2_STT**	**7:0**	**Default : 0x04**	**Access : R/W**
	OUT_INV	7	Output Inverse.	
	OEV2_STT_MULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_OEV2_STT[4:0]	4:0	OEV2 pulse Start.	
EAh	**GPO_OEV3_STT**	**7:0**	**Default : 0x04**	**Access : R/W**
	OUT_INV	7	Output Inverse.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	OEV3_STT_MULT [1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_OEV3_STT[4:0]	4:0	OEV3 pulse Start.	
EBh	**HSTT_DLY_L**	**7:0**	**Default :0x04**	**Access : R/W**
	HSTT_DLY[7:0]	7:0	H Start Delay numbers Low byte.	
ECh	**HSTT_DLY_H**	**7:0**	**Default :0xA4**	**Access : R/W**
	EXT_DIS_RNG	7:4	Extraction start point in line extraction mode.	
	-	3	Reserved.	
	HSTT_DLY_EN	2	H Start Delay Enable.	
	HSST_DLY[9:8]	1:0	H Start Delay numbers High byte.	
EDh	**CLK_DLY_SYNCOUT**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRPSETH	7	Set High to Invert RGB Data when FRP Disable (BK1_D2[1]=1).	
	-	6	Reserved.	
	TC_GPIO_SEL	5	0: TC function. 1: GPIO function.	
	OEV_MD_SEL	4	0: Normal mode. 1: Special mode.	
	CLK_DLY_SEL_TC [3:0]	3:0	TCCLK Delay Select.	
EEh	**GPO_CKV_END2**	**7:0**	**Default : 0x28**	**Access : R/W**
	CKV2_EN	7	CKV2 Enable.	
	CKV_END2_MULT[1:0]	6:5	00: x1. 01: x4. 10: x8. 11: x16.	
	GPO_CKV_END2	4:0	CKV2 End point.	
EFh	**Q1H_SETTING**	**7:0**	**Default : 0x08**	**Access : R/W**
	Q1H_ENABLE	7	Q1H output from SEQ_MODE pin, toggle point is using OEV3 signal start point.	
	TCCLK_INV_MODE	6:3	0001: TCCLK invert every field. 0011: TCCLK invert when Q1H is high. 0101: TCCLK invert when Q1H and field are high. 1001: TCCLK invert when Q1H is low and field is high.	
	-	2	Reserved.	
	INTOUT_OEN	1	Testmode. PAD_INTOUT output enable control. 0: Output. 1: Input.	
	CLKIN_SEL	0	Testmode External Clock Select. 0: PAD_INTOUT. 1: PAD_CLKIN.	

Analog Register (Bank = 01)

Index	Name	Bits	Description	
F0h	**WDT0**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_TESTMD	7	CSOG test mode for WDT counter.	
	WDT_LD	6	Watch Dog Timer Load Value by SW.	
	WDT_EN	5	Watch Dog Timer Enable Bit.	
	-	4:0	Reserved.	
F1h	**WDT1**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_WIDTH	7:0	Watch Dog Timer Width.	
F2h	**WRLOCK0**	**7:0**	**Default : 0x00**	**Access : R/W**
	WRLOCK0	7	Register lock (work with WRLOCK1). Register access is disabled when WRLOCK0 and WRLOCK1 are HIGH. Register access is enabled when WRLOCK0 and WRLOCK1 are LOW.	
	-	6:0	Reserved.	
F3h	**PWMCLK**	**7:0**	**Default : 0x00**	**Access : R/W**
	DB_EN	7	Double Buffer Enable. 0: Disable. 1: Enable.	
	P2REN	6	PWM2 Reset every frame Enable. 0: Disable. 1: Enable.	
	P1REN	5	PWM1 Reset every frame Enable. 0: Disable. 1: Enable.	
	P2POL	4	PWM 2 Polarity when enhance PWM2 enable.	
	EP2EN	3	Enhance PWM2 Enable. 0: Disable. 1: Enable.	
	P1POL	2	PWM1 Polarity when enhance PWM1 enable.	
	EP1EN	1	Enhance PWM1 Enable. 0: Disable. 1: Enable.	
	PCLK	0	PWM1/2 base Clock select. 0: 14.318MHz. 1: 14.318MHz / 4.	
F4h	**PWM1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_POL	7	PWM1 polarity.	
	PWM1_CTUN[6:0]	6:0	PWM1 Coarse adjustment.	
F5h	**PWM2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_POL	7	PWM2 polarity.	
	PWM2_CTUN[6:0]	6:0	PWM2 Coarse adjustment.	
F6h	**PWM1EPL**	**7:0**	**Default : 0x00**	**Access : R/W**
	EPWM1P[7:0]	7:0	Enhance PWM1 Period.	
F7h	**PWM1EPH**	**7:0**	**Default : 0x00**	**Access : R/W**

Analog Register (Bank = 01)

Index	Name	Bits	Description	
	EPWM1P[15:8]	7:0	Enhance PWM1 Period.	
F8h	**PWM2EPL**	**7:0**	**Default : 0x00**	**Access : R/W**
	EPWM2P[7:0]	7:0	Enhance PWM2 Period.	
F9h	**PWM2EPH**	**7:0**	**Default : 0x00**	**Access : R/W**
	EPWM2P[15:8]	7:0	Enhance PWM2 Period.	
FAh ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

Video Decoder Register (Bank = 02)

Video Decoder Register (Bank = 02)				
Index	**Name**	**Bits**	**Description**	
01h	**STATUS1**	**7:0**	**Default : -**	**Access : RO**
	READBUS1	7:0	Test bus 1.	
02h	**STATUS2**	**7:0**	**Default : -**	**Access : RO**
	READBUS2	7:0	Test bus 2.	
03h	**STATUS3**	**7:0**	**Default : -**	**Access : RO**
	READBUS3	7:0	Test bus 3.	
04h	**STATUS_MUX**	**7:0**	**Default : 0x00**	**Access : R/W**
	READBUS_CTRL	7:0	VIPTESTMUX Address Control of READBUS1, READBUS2, and READBUS3.	
05h ~ 06h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
07h	**DSP_ADD_PRT**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSP_ADD_PRT[7:0]	7:0	DSP register Address Port.	
08h	**DSP_WDAT_PRT**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSP_WDAT_PRT[7:0]	7:0	DSP register Write Data Port.	
09h	**DSP_RDAT_PRT**	**7:0**	**Default : -**	**Access : RO**
	DSP_RDAT_PRT[7:0]	7:0	DSP register Read Data Port.	
10h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
11h	**COMB_LL_EN**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	APL_COMB_LL_EN	0	1: Mux to select Com Line Lock mode.	
12h ~ 13h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
14h	**SOFT_RST**	**7:0**	**Default : 0x10**	**Access : R/W**
	SOFT_RST	7	1: Softrest AFEC modules.	
	-	6:0	Reserved.	
15h	**FPGA_CTRL**	**7:0**	**Default : 0xA8**	**Access : R/W**
	FPGA_CTRL	7:0	Reserved for FPGA control.	
16h	**REG_SOFT_RST2**	**7:0**	**Default : 0x00**	**Access : R/W**
	REG_SOFT_RST2	7:0	Reserved for HW testing.	
17h	**CLK_CTRL**	**7:0**	**Default : 0xC9**	**Access : R/W**
	FSCPLL_MODE	7	0: External FSC Clock Mode. 1: Internal FSC Clock Mode.	
	ADC_DOUBLE	6	ADC Double Sample Rate Option.	
	REG_CLK_VD_VIP	5:4	00: 4 Fsc Clock on Digital. 11: 8 Fsc Clock on Digital.	

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	REG_VCO_TYPE	3:2	10: VCO 16 Fsc. 01: VCO 8 Fsc. 00: VCO 4 Fsc.	
	REG_ADC_CLK_LAG	1:0	CLK_CC / CLK_ADC Phase Diff.	
18h	**CSTATE_CTRL**	**7:0**	**Default : 0x86**	**Access : R/W**
	CTRL_MD	7:5	Default: 100b, Auto control mode.	
	-	4	Reserved.	
	CTRL_STATE	3:0	State Stable State Value; default: 0110b.	
19h	**MVDET_EN**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MV_DETEC_EN	7	Microvision Detect Enable. 0: Disable. 1: Enable.	
	-	6:5	Reserved.	
	DSP_SYNC_ALW	4	Allow DSP to Control SYNC_FOUND.	
	DSP_APL_ALW	3:2	0: Allow DSP to Control APL_FREQ_IDEAL (Center Frequency).	
	SECAM_MD	1:0	1: Allow DSP to Control APL_FREQ and APL_PHS (Full frequency/PHS control).	
1Ah	**SVD_EN**	**7:0**	**Default : 0x40**	**Access : R/W**
	SVIDEO_EN	7	0: Chroma Source from CVBS-Channel Input. 1: Chroma Source from C-Channel Input.	
	ADC_C_ALWY_ON	6	Chroma ADC 16Fsc-to-4Fsc Down-Sampling is Enabled.	
	CLAMDSM_CTRL[15:10]	5:0	Clamping 12-bit Control code; integer parts.	
1Bh	**BKLVL_FORCE1**	**7:0**	**Default : 0x80**	**Access : R/W**
	DISCLAMP3	7	HW Clamping frozen 3 times if SYNC magnitude is small.	
	CLMP_FREZ_ZERO	6	HW Clamping set to Zero when Frozen.	
	CLAMDSM_CTRL[9:4]	5:0	Clamping 12-bit control code; fractional parts.	
1Ch	**BKLVL_FORCE2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CLMFZE_VRGE	7:0	Clamp Freeze of V Range.	
1Dh	**VCR_VLSHT**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CLMFZE_HRGE	7:0	Clamp Freeze of H Range.	
1Eh	**DSP_EN**	**7:0**	**Default : 0x80**	**Access : R/W**
	DSP_EN_SYS	7	1: Enable SW DSP Function.	
	-	6:0	Reserved.	
1Fh	**CLMP_C_EN**	**7:0**	**Default : 0x60**	**Access : R/W**
	CLMP_C_EN	7	2nd ADC Chroma Clamping Enable.	
	CLMP_K1_INI	6:0	HW Clamping K1 when system not stable.	
20h	**APLL_CTRL1**	**7:0**	**Default : 0xBC**	**Access : R/W**
	APL_EN	7	Analog burst-lock PLL Enable.	
	APL_TYPE	6:4	APL Type.	
	-	3:2	Reserved.	

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	APL_EN2	1	No state 7, when no bust.	
	CLMP_6B_FORCE	0	Clamp value 6-bit test mode enable.	
21h	**APLL_CTRL2**	**7:0**	**Default : 0x18**	**Access : R/W**
	CLMP_2DSM	7	Second order Clamp method.	
	APL_COMB_LL_TST[1]	6	0: Comb-Line-Lock Disabled if VCR. 1: Com-Line-Lock Enabled even for VCR.	
	APL_COMB_LL_TST[0]	5	0: Fractional SYNC Phase is used. 1: Integer PD from Comb.	
	DPL_PHS_CAL	4	DPL Phase Calibration.	
	APL_CEZANNE	3	For CEZANNE FPGA Test.	
	PALSWH_MODE	2:1	PAL Switch Mode control.	
	APL_COMB_LL_EN	0	Comb Line-Locked mode Enable.	
22h	**APL_FREQ_MD**	**7:0**	**Default : 0x61**	**Access : R/W**
	APL_FREQ_MD[7:5]	7:5	APL Freq Mode.	
	-	4:3	Reserved.	
	ACLPZ_WDTH	2:0	Clamping Width.	
23h	**APLL_TRANGE**	**7:0**	**Default : 0x40**	**Access : R/W**
	APL_FREQ_LMT	7:5	Burst PLL Frequency Limitation. 0: 125ppm. 2: 250ppm. 4: 500ppm. 6: 1000ppm.	
	-	4:1	Reserved.	
	APL_K_FORCE	0	APL K value Force enable.	
24h	**APL_K1_NOISY**	**7:0**	**Default : 0x04**	**Access : R/W**
	APL_K1_NOISY[7:0]	7:0	APLL phase tracking coefficients for Noisy broadcast.	
25h	**APL_K2_NOISY**	**7:0**	**Default : 0x02**	**Access : R/W**
	APL_K2_NOISY[7:0]	7:0	APLL frequency tracking coefficients for Noisy broadcast.	
26h	**APL_K1_NORM**	**7:0**	**Default : 0x10**	**Access : R/W**
	APL_K1	7:0	APLL phase tracking coefficients for normal condition.	
27h	**APL_K2_NORM**	**7:0**	**Default : 0x08**	**Access : R/W**
	APL_K2	7:0	APLL frequency tracking coefficients for normal condition.	
28h	**APL_K1_VCR**	**7:0**	**Default : 0x02**	**Access : R/W**
	APL_K1_VCR	7:0	APLL phase tracking coefficients for VCR.	
29h	**APL_K2_VCR**	**7:0**	**Default : 0x01**	**Access : R/W**
	APL_K2_VCR	7:0	APLL frequency tracking coefficients for VCR.	
2Ah	**MODE_PFSC**	**7:0**	**Default : 0x20**	**Access : R/W**
	MD_PFSC[7]	7	0: Auto Fsc. 1: Manual Fsc.	

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	MD_PFSC[6:4]	6:4	When bit[7]=1, 000: fsc=4.43361875 MHz. 001: fsc=4.406 MHz. 010: fsc=3.579545 MHz. 100: fsc=3.57561149 MHz. 110: fsc=3.58205625 MHz.	
	VDFD_ASWFSC	3	Internal blind FSC try.	
	VDFD_ASWFSC1	2	Internal blind FSC try1.	
	HALFWIN_OP	1	Half Window period Option. 0: Asserted between 1/4 to 3/4 line period. 1: Asserted between 1/2 to 1 line period.	
	OEINV_MD	0	ODD_EVEN_INVERT bit inversion Mode. 0: Directly bypass. 1: Inverse.	
2Bh	**VDFD_CTRL1**	**7:0**	**Default : 0x7E**	**Access : R/W**
	VDFD_FD_L	7:4	Fast attack frequency tracking time period.	
	VDFD_PHSSTD_L	3:0	Monitor Phase tracking time period.	
2Ch	**VDFD_CTRL2**	**7:0**	**Default : 0x67**	**Access : R/W**
	PHS_DIFF_THRD	7:4	Phase tracking deviation large Threshold.	
	PHS_STD_RANGE	3:0	Phase tracking deviation small threshold.	
2Dh	**FD_K**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FD_K	7:4	Fast Attack Frequency Tracking Coefficient.	
	APL_PHS_OFST[11:8]	3:0	Preferred Phase Offset of the Analog Burst-locked PLL.	
2Eh	**APL_PHS_OFST**	**7:0**	**Default : 0x00**	**Access : R/W**
	APL_PHS_OFST[7:0]	7:0	Preferred Phase Offset of the analog burst-locked PLL.	
2Fh	**BLACK_SEL**	**7:0**	**Default : 0x24**	**Access : R/W**
	SETUP_YES	7:5	0x: Based on confirm mode auto determine. NTSC: setup. PAL: no setup. 10: Force no setup for NTSC. 11: Force setup for PAL.	
	-	4:2	Reserved.	
	-	1:0	Reserved.	
30h	**CLAMP_CTRL**	**7:0**	**Default : 0x01**	**Access : R/W**
	CLAMPDAC_CTRL[7:6]	7:6	00: Auto clamping control. 01: Auto clamping control, but polarity inverted. 10: Force clamping control by bit[5:0]. 11: Auto clamping control.	
	CLAMPDAC_CTRL[5:0]	5:0	Clamping control value.	
31h	**CLAMP_COEF1**	**7:0**	**Default : 0x40**	**Access : R/W**
	CLMP_TYPE_ST3BOT	7	CLMP_BOT function enable in STAE3.	

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	CLMP_K1	6:0	Clamping speed; the larger the faster. 7'b101_1000 suggested for 1.00 uF. 7'b100_0000 suggested for 0.10 uF. (default) 7'b010_1000 suggested for 0.01 uF.	
32h	**CLAMP_COEF2**	**7:0**	**Default : 0xA0**	**Access : R/W**
	CLMP_TYPE	7	Back-porch clamping enable (default =1).	
	CLMP_K2	6:0	Leakage current tracking speed. Smaller value is preferred. 7'b001_0000 suggested for 1.00 uF. 7'b010_0000 suggested for 0.10 uF. (default). 7'b011_0000 suggested for 0.01 uF.	
33h	**CLAMP_COEF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLMP_LKG_MODE	7:4	Leakage control Mode.	
	ADCLOSS_CNT	3:0	Count value of ADC Loss status.	
34h	**CLAMP_COEF4**	**7:0**	**Default : 0x82**	**Access : R/W**
	CLMP_BOTSPD	7:6	Bottom reference LPF selection.	
	CLMP_DLKG_MAC	5:0	Delta leakage is bounded by +- (CLAMP_DLKG_MAX/512).	
35h	**CLAMP_REF_SEL1**	**7:0**	**Default : 0x0A**	**Access : R/W**
	BLANKLVL_CTRL	7	Blank Level Control.	
	BLANK_LVL[8]	6	Blank Level bit[8].	
	CLMP_LKG	5:0	If CLAMP_LKG_MD = 1011, leakage is forced by CLAMP_LKG[4:0] * sign; where, sign=+1 if bit[5]=1, and sign=-1 if bit[5]=0. Default: 6'd10.	
36h	**CLAMP_COEF5**	**7:0**	**Default : 0x45**	**Access : R/W**
	CLMP_BOTSEL	7:5	Clamp Bot Selection enable.	
	CLMP_ERR_MAX	4:0	Back porch level Error for clamping is bounded by +- CLMP_ERR_MAX*8 (Default: 5'd25).	
37h	**CLAMP_REF_SEL2**	**7:0**	**Default : 0xF0**	**Access : R/W**
	BLANK_LVL[7:0]	7:0	Blank Level.	
38h	**VSTROBE_LIMIT**	**7:0**	**Default : 0x13**	**Access : R/W**
	BLACKLVL_CTRL	7	Black Level Control.	
	BLACK_LVL[8]	6	Black Level bit[8].	
	HV_VCNTSEL	5	1: Enable 2nd Integration Protection for V Extraction.	
	HV_VLINPROT	4	0: Enable Next V Extraction after 50 Lines. 1: Enable Next V Extraction after 200 Lines.	
	BOTAV_INSEL	3	Bottom of active video Input Selection.	
	BOT_INSEL	2:0	Bottom of whole line Input Selection.	
39h	**VSTROBE_PROTECT**	**7:0**	**Default : 0x6C**	**Access : R/W**
	WP_INSEL	7:5	Sync Input LPF BW Selection.	
	HV_INSEL	4:2	HSYNC/VSYNC slicer level Selection.	
	TOP_INSEL	1:0	Top level Input Selection.	
3Ah	**BLACK_LVL**	**7:0**	**Default : 0xCC**	**Access : R/W**

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	BLACK_LVL[7:0]	7:0	Black Level value.	
3Bh	**HV_VEXTH**	**7:0**	**Default : 0x7D**	**Access : R/W**
	HV_VEXTH	7:0	0: V Extract by Line Length Unit. 1: V Extract by Manual Pixel Length Units.	
3Ch	**HV_C TRL1**	**7:0**	**Default : 0x2A**	**Access : R/W**
	HV_VSEL	7:6	00: V Extract native. 01: V Extrat Native Synchronize to next line start/middle. Other reserved.	
	HV_VTHRDSEL	5:4	00: 3/8 line. 01: 6/8 line. 10: 1.25 line. 11: 1.75 line. As Threshold for V Extract.	
	HV_INTCNT	3:0	Composite SYNC Pixel Lengths Filter for V Extract.	
3Dh	**V_POSTCOAST**	**7:0**	**Default : 0x00**	**Access : R/W**
	VCOST_FEXT	7:6	Coast forward control.	
	VCOST_BEXT	5:0	Coast Backward control.	
3Eh	**HV_SLICTRL**	**7:0**	**Default : 0x0C**	**Access : R/W**
	HV_SLICTRL	7:0	HSYNC/VSYNC Slicer Control.	
3Fh	**HV_HSLIOFSTHYS**	**7:0**	**Default : 0xC0**	**Access : R/W**
	HV_HSLIOFSTHYS	7:4	HSYNC slicer line Offset.	
	AGC_FINE_LSB	3:0	AGC Fine gain (lower 4 bits).	
40h	**PGA_CTRL1**	**7:0**	**Default : 0xC1**	**Access : R/W**
	PGA_AUTO	7	0: Manual PGA set by AGC_COARSE[1:0]. 1: Auto PGA switch.	
	PGA_FSWT	6	0: PGA switch in VSYNC. 1: PGA switch in HSYNC.	
	AGC_COARSE	5:4	00: PGA x 1. 01: PGA x 2.	
	FREZ_CLMPDISBK	3	Freeze Clamp Function; VSYNC selection.	
	SYNC_MAG_LOW_TH	2:0	If SYNC Magnitude is Low, Freeze HW Clamping 3 times.	
41h	**PGH_TOP_TH**	**7:0**	**Default : 0xDA**	**Access : R/W**
	PGA_TH_TOP	7:0	If AGC_FINE[11:0]>=16*PGA_TH_TOP[7:0], use smaller PGA and 16*PGA_H2L[7:0].	
42h	**PGA_BOT_TH**	**7:0**	**Default : 0x40**	**Access : R/W**
	PGA_TH_BOT	7:0	If AGC_FINE[11:0]<=16*PGA_TH_BOT[7:0], use larger PGA and 16*PGA_L2H[7:0].	
43h	**AGC_CTRL1**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7	Reserved.	

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	AGC_MD	6:5	00: Auto, REG_AGC_K used for both search and lock. 01: Auto, REG_AGC_K used for search, clipping delta-gain=-1, 0, +1 for lock. 10: Freeze gain. 11: Load gain=AGC_FINE*16. Default=1.	
	AGC_LOCK_CTRL	4	AGC Lock Control.	
	AGC_TYPE	3:2	00: Sync. 01: Sync. 10: Color bust. 11: Hybrid of 1 and 2. Default=1, HSYNC as primary reference, color burst is for ACC.	
	AGC_LOWTH_PGA	1:0	During PGA switching, PGA must be larger than AGC_LOWTH_PGA.	
44h	**AGC_FINE**	**7:0**	**Default : 0xC0**	**Access : R/W**
	AGC_FINE	7:0	Used when AGC_MODE=11.	
45h	**AGC_CTRL2**	**7:0**	**Default : 0x42**	**Access : R/W**
	AGC_AVGL	7:5	AGC average lines=2^(AGC_AVGL + 1).	
	-	4	Reserved.	
	AGC_WAITL	3:1	Lines to wait for analog settling down=2^(AGC_WAITL) after each gain update.	
	-	0	Reserved.	
46h	**AGC_K_CTRL**	**7:0**	**Default : 0x73**	**Access : R/W**
	AGC_K_FAST	7:4	Fast-attack AGC update speed. Delta_gain=+-(AGC_K_FAST*4+3)/256*gain_true.	
	AGC_K	3:0	Sync magnitude AGC update speed. Delta_gain=amp_err/256*(1+ AGC_K)/32*gan_true.	
47h	**AGC_CTRL3**	**7:0**	**Default : 0x3F**	**Access : R/W**
	AGC_BKLCLIP	7:5	AGC Black level Clip enable.	
	AGC_CLIP	4:0	The sync magnitude error for AGC is bounded by +-4*REG_AGC_CLIP.	
48h	**PGA_SWTICH_TH1**	**7:0**	**Default : 0xC0**	**Access : R/W**
	PGA_L2H	7:0	Used when AGC_FINE<=PGA_TH_BOT*16. Default: 3072/16=8'd192.	
49h	**PGA_SWCH_TH2**	**7:0**	**Default :**	**Access : R/W**
	PGA_H2L	7:0	Used when AGC_FINE<=PGA_TH_BOT*16. Default: 1238/16 = 8'd64.	
4Ah	**AGC_LOWTH**	**7:0**	**Default : 0xA0**	**Access : R/W**
	AGC_LOWTH	7:0	When PGA=AGC_LOWTH_PGA, AGC_FINE[11:0] must be smaller than 16*AGC_LOWTH.	
4Bh	**PGA_OFST**	**7:0**	**Default : 0x40**	**Access : R/W**
	PGA_OFST	7:0	ADC VREF offset=VREF_min/(VREF_max-VREF_min)*4096/16.	
4Ch	**BRST_WINDOW1**	**7:0**	**Default : 0x62**	**Access : R/W**
	BRST_MASK_0	7:5	HSYNC trailing edge trasition region Maskout for Burst Calculation.	

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	BRST_BEG	4:0	Burst window Beginning position; move to SW.	
4Dh	**BRST_WINDOW2**	**7:0**	**Default : 0x40**	**Access : R/W**
	BRST_END	7:0	Burst window End position; move to SW.	
4Eh	**BK_WINDOW1**	**7:0**	**Default : 0x05**	**Access : R/W**
	BKPRH_CTR[8]	7	Back-Porch Window Center Position.	
	BKPRH_SEL	6	Back-Porch Selection.	
	BKPRH_AUTSW	5:4	Back-Porch Auto Switch.	
	BKPRH_WIN	3:0	Back-porch Window width=(*4+4).	
4Fh	**BK_WINDOW2**	**7:0**	**Default : 0x68**	**Access : R/W**
	BKPRH_CTR[7:0]	7:0	Back-Porch Window Center Position.	
50h	**BRST_TH**	**7:0**	**Default : 0x80**	**Access : R/W**
	BRST_THRD	7:4	Burst Threshold.	
	BRST_AMP_THRD	3:0	Burst found Amplitude Threshold.	
51h	**BRSTMAG_CTRL**	**7:0**	**Default : 0x38**	**Access : R/W**
	BRSTMAG_CTRL	7	Burst Magnitude Control.	
	BRST_MAG[8:2]	6:0	Burst Magnitude value.	
52h	**COMB_LL_CTRL**	**7:0**	**Default : 0x04**	**Access : R/W**
	BRST_MAG[1:0]	7:6	Burst Magnitude value.	
	-	5:4	Reserved.	
	PAL_BLIND_PD_EN	3	NTSC; 180 degree Phase Detection Enable.	
	BRST_PHS_CHK_MAG	2	Burst Phase of the current line is ignored if BRST_MAG<BRST_MAG_AVG/8.	
	-	1:0	Reserved.	
53h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
54h	**BRST_WINDOW3**	**7:0**	**Default : 0x23**	**Access : R/W**
	FSC_THRD_LINES	7:5	FSC Threshold Lines.	
	-	4:3	Reserved.	
	FSC_TST_TRY[2]	2	Fsc selection 1.25*Fsc and 0.8*Fsc BPF magnitude type.	
	FSC_TST_TRY[1]	1	Fsc selection 1.0*Fsc BPF magnitude type.	
	FSC_TST_TRY[0]	0	Fsc selection BPF magnitude snapshop taken at the end of the burst window.	
55h	**COLOR_OFF**	**7:0**	**Default : 0x08**	**Access : R/W**
	KILL_CSPOUT	7:6	00 or 01: Auto Color Kill. 10: Force Show Color. 11: Force Kill Color.	
	-	5	Reserved.	
	PAL_LINES_TH	4:0	Lines for PAL/NTSC detection=64 * PAL_LINES_TH.	
56h	**FSC443/357 DECT1**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	

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Index	Name	Bits	Description	
	FSC_THRD1_PASS	5:0	FSC Threshold1 Pass.	
57h	**FSC443/357 DECT2**	**7:0**	**Default : 0x28**	**Access : R/W**
	-	7:6	Reserved.	
	FSC_THRD1_FAIL	5:0	FSC Threshold1 Fail.	
58h	**FSC443/357 DECT3**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	FSC_THRD0_PASS	5:0	FSC Threshold0 Pass.	
59h	**FSC443/357 DECT4**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	FSC_THRD0_FAIL	5:0	FSC Threshold0 Fail.	
5Ah	**BRST_UNKNOW_TH**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	FSC_TST_MASK	6:4	HSYNC trailing edge Trasition region Maskout for Fsc selection filters.	
	FSC_THRD_NO_BRST	3:0	FSC Threshold for No Burst detection.	
5Bh	**FSC443/357 DECT5**	**7:0**	**Default : 0x98**	**Access : R/W**
	FSC_THRD_MAG_HYST[3:2]	7:6	FSC Threshold Magnitude of HSYNC start.	
	FSC_THRD_MAG_443	5:0	FSC Threshold Magnitude of 4.43 MHz.	
5Ch	**FSC443/357 DECT6**	**7:0**	**Default : 0x98**	**Access : R/W**
	FSC_THRD_MAG_HYST[1:0]	7:6	FSC Threshold Magnitude of HSYNC start.	
	FSC_THRD_MAG_358	5:0	FSC Threshold Magnitude of 3.58 MHz.	
5Dh	**ACC_CTRL**	**7:0**	**Default : 0x08**	**Access : R/W**
	ACC_CTRL	7:6	Auto Chroma Control. 01: Reset Chroma_Gain=1. 11: Load Chroma_Gain=ACC_GAIN[13:0]/64.	
	ACC_GAIN[5:0]	5:0	Auto-Chroma-Control Gain.	
5Eh	**ACC_GAIN**	**7:0**	**Default : 0x20**	**Access : R/W**
	ACC_GAIN[13:6]	7:0	Auto-Chroma-Control Gain.	
5Fh	**AGC_DELTA**	**7:0**	**Default : 0x28**	**Access : R/W**
	AGC_DELTA[7:5]	7:5	AGC Delta value.	
	WP_SIM_SPD	4:3	WP Simulation Speedup.	
	WP_LVL_SPD	2:0	WP Level Speedup.	
60h	**WP_CTRL1**	**7:0**	**Default : 0x15**	**Access : R/W**
	ACC_C_PEAK_LPF	7:6	Chroma Peak Detection Update Speed. 00: Slow, Narrow-Band-Width. 11: Fast, Wide-Band-Width.	
	-	5	Reserved.	
	WP_TH[8]	4	Desired white level=512+REG_WP_TH.	

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Index	Name	Bits	Description	
	AGC_K_WP	3:0	White peaking AGC update speed. Delta_gain=white_err/256*(1+REG_AGC_K)/ 32*gain_true.	
61h	**WP_THRD**	**7:0**	**Default : 0x24**	**Access : R/W**
	WP_THRD[7:0]	7:0	White Peak Threshold value.	
62h	**AP_SYNTHRD2REAGC**	**7:0**	**Default : 0x78**	**Access : R/W**
	WP_SYNTHRD2REAGC	7:0	WP Sync Threshold of AGC.	
63h ~ 64h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
65h	**AGC_CTRL4**	**7:0**	**Default : 0x55**	**Access : R/W**
	-	7:2	Reserved.	
	WP_WAITTH	1:0	Number of sync-mag AGC operations before WP mode. 00: 255 operations. 01: 127 operations. 10: 63 operations. 11: 31 operations.	
66h	**WP_CTRL2**	**7:0**	**Default : 0x70**	**Access : R/W**
	WP_MODE	7:5	0xx: Internally automatic white-peaking control. 100: Disable white-peaking. 101: Hold sync magnitude AGC if white level is too high. 110: Reserved. 111: Normal white-peaking AGC.	
	WP_MONTR_SPD	4:2	WP Monitor Speed.	
	ADCOVSLE_THRD	1:0	WP Threshold Selection.	
67h	**WP_REDO**	**7:0**	**Default : 0x17**	**Access : R/W**
	ROUND_CTRL	7:5	AFEC signal rounding selection.	
	REMOV_HF_NOISE	4	Enable 13-tap CVBS low-pass filter to Remove High-Frequency Noise.	
	ROUND_CTRL[3:2]	3:2	7-tap chroma-trap filter, CCTRAP, Rounding. 00: Truncate. 01: Round. 10: Dither.	
	ROUND_CTRL[1]	1	AFEC self-test 1D luminance Rounding. 0: Truncate. 1: Round.	
	ROUND_CTRL[0]	0	AFEC self-test 1D chroma Rounding. 0: Truncate. 1: Round.	
68h	**CLK_CTRL1**	**7:0**	**Default : 0x45**	**Access : R/W**
	ADC_84_ROUND	7:6	Round control for 8Fsc-to-4Fsc downsampling. 0: Truncate. 1: Round.	
	DAC_LATCH_INV	5	Option for Datalatch from 4Fsc to 8Fsc.	

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	3DAC_EN	4	Enable AFEC Data Output to DAC.	
	FILSEL	3:2	Filter Selection.	
	ADC_168_ROUND	1:0	Round Control for 16Fsc-to-8Fsc Downsampling. 0: Truncate. 1: Round.	
69h	**SRC_CTRL1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SELYC	7	0: YC Source from AFEC for Testing Purpose. 1: YC Source from Comb for Display.	
	-	6:5	Reserved.	
	BYPASS_Y	4	Bypass CVBS Source for Testing purpose.	
	COMB601H_SYNC	3	1: Use the HS444 as the MVDA_HS Output.	
	COMB601V_SYNC	2	1: Use the VS444 as the MVDA_VS Output.	
	COMB601F_SYNC	1	1: Use the Fld444 as the MVDA_F Output.	
	COMBPASS_SYNC	0	1: The HS444 and VS444 as the Bypass SYNC. 0: AFEC_HS and AFEC_VS as the Bypass SYNC Output.	
6Ah	**VCR_DETECT1**	**7:0**	**Default : 0x51**	**Access : R/W**
	VCR_MODE	7:6	VCR Mode enable.	
	VCR_HD_DLY	5:4	VCR Head switch number.	
	-	3	Reserved.	
	VS_STB	2:0	VS Strobe.	
6Bh	**VCR_DETECT2**	**7:0**	**Default : 0xAA**	**Access : R/W**
	VCR_LDT	7:4	VCR Line Margin.	
	FAST_VT_DET	3	Fast Vertical Line Detection.	
	VCR_THRD	2:0	VCR Threshold.	
6Ch	**VCR_PRECOAST**	**7:0**	**Default : 0xF0**	**Access : R/W**
	VCR_PRECOAST	7:4	Pre-Coast value for VCR mode.	
	HV_HSLISEL_VCR	3:2	HSYNC Slicer Selection for VCR mode.	
	HV_SLILOW_SEL	1:0	HSYNC/VSYNC slicer Low Selection.	
6Dh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
6Eh	**VCR_VLSET**	**7:0**	**Default : 0x14**	**Access : R/W**
	VCR_VLSET	7:0	PAC/NTSC VLine tunning.	
6Fh		**7:0**	**Default :**	**Access :**
	RST_AFEC_SEL	7	0: Partial reset AFEC. 1: Global reset AFEC.	
	-	6:4	Reserved.	
	DPL_DDE_EN	3	DPL double DE Enable.	
	DDE_EN	2	Double DE Enable.	
	DPL_HS_EN	1	DPL HS Enable.	
	DPL_DE_EN	0	DPL DE Enable.	
70h	**INI_CTRL1**	**7:0**	**Default : 0x84**	**Access : R/W**

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	FSTAGC_EN	7	Fast AGC mode.	
	-	6	Reserved.	
	CLMP_BOTMD	5:4	Clamp on Bottom Mode.	
	ADSMAL_THRD	3:0	Threshold for detecting Small AOC swing.	
71h	**BOTREF_LVL**	**7:0**	**Default : 0xA0**	**Access : R/W**
	BOTREF_LVL	7:0	Bottom Reference Level.	
72h	**HV_SLC_CTRL**	**7:0**	**Default : 0x37**	**Access : R/W**
	HV_SLCFZE	7:6	HSYNC/VSYNC Slice Freeze control.	
	HV_SLCDIF	5:4	HSYNC/VSYNC Slice Difference.	
	HV_SLCDLT	3:0	HSYNC/VSYNC Slice Limit.	
73h	**INI_CTRL1**	**7:0**	**Default : 0x52**	**Access : R/W**
	HV_VSLISEL	7:6	00: 2/8 syn_magnitude as hslice level. 01: 4/8 syn_magnitude as hslice level. 10: 5/8 syn_magnitude as hslice level. 11: 6/8 syn_magnitude as hslice level.	
	HV_HSLISEL	5:4	00: 2/8 syn_magnitude as vslice level. 01: 4/8 syn_magnitude as vslice level. 10: 5/8 syn_magnitude as vslice level. 11: 6/8 syn_magnitude as vslice level.	
	656_HDES_VCR_OFST	3:0	656 SAV Position Offset when VCR.	
74h	**SLICE_MUX**	**7:0**	**Default : 0x97**	**Access : R/W**
	SLICE_MUX	7:0	Slicer level selection.	
75h	**656_OFST**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	656_OFST	6:0	56 SAV Position Offset in VCR mode.	
76h	**656_CTRL1**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	DBCLK_TEST	4	Clock Testing.	
	-	3	Reserved.	
	656_BLNK_MD	2	656 Blank Mode.	
	656_EN	1	Enable 656 mode.	
	ABNML_CHK	0	Abnormal check enable.	
77h	**656_BLNK_MAX**	**7:0**	**Default : 0x02**	**Access : R/W**
	656_BLNK_MAX[7:0]	7:0	656 Blink Max value.	
78h	**YUV**	**7:0**	**Default : 0x00**	**Access : R/W**
	YUV[7:0]	7:0	Used as Input of the 4Fsc-to-16Fsc Up-sampling if SELUPS=3.	
79h	**656_HDES1**	**7:0**	**Default : 0x18**	**Access : R/W**

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	656_HDES_O[9:2]	7:0	SDA start position. (656_HDESM, 656_HDESL) ITU656 SAV Position. For VCR, 656_HDES=656_HDES_o-656_HDES_VCR_OFST*4. Otherwise, 656_HDES=656_HDES_o.	
7Ah	**656_HDES2**	**7:0**	**Default : 0x20**	**Access : R/W**
	656_HDES_O[1:0]	7:6	ITU656 SAV position.	
	-	5:2	Reserved.	
	656_INV_F	1	656 Field Inverse.	
	-	0	Reserved.	
7Bh	**656_HDEW**	**7:0**	**Default : 0xB3**	**Access : R/W**
	656_HDEW	7:0	ITU656 active data Width (*8+7).	
7Ch	**SLMIS_CTRL**	**7:0**	**Default : 0xC0**	**Access : R/W**
	SLMIS_CTRL[7:0]	7:0	Enable Slice Miss freeze.	
7Dh	**NOISE_MLINE**	**7:0**	**Default : 0x04**	**Access : R/W**
	NOISE_MLINE	7:0	Move Noise level during specify Line Number.	
7Eh	**656_CTRL2**	**7:0**	**Default : 0x80**	**Access : R/W**
	656_CLKINV	7	Used for FPGA testing.	
	656_CLKDLY	6:5	Used for FPGA testing.	
	656_LSTSEL	4	Used for FPGA testing.	
	656_TEST	3:2	Used for FPGA testing.	
	TEST_MODE	1:0	Used for FPGA testing.	
7Fh	**444_VD_CTRL**	**7:0**	**Default : 0x62**	**Access : R/W**
	SELDAC	7:6	Source for 3 DACs. 00: Comb. 01: AFEC Test Mode. 10: 444. 11: Upsampling Source.	
	3DAC_INSHV	5	Insert HV into Display DAC Source.	
	3DAC_HSEL	4	Insert H's Source Selection. 0: Window PLL. 1: Display PLL.	
	3DAC_INSBLACK	3	Insert Black Level back to DAC Source.	
	REG_SELFB	2	0: YCbCr Source from AFEC Test Mode. 1: YCbCr Source from Comb444.	
	REG_SELUPS	1:0	Upsampling Source. 10: Test Mode 444. 11: Comb YCbCr 444.	
80h	**NCO_FSC0**	**7:0**	**Default : 0x48**	**Access : R/W**
	FSC_NCO0[23:16]	7:0	{NCO_FSC0} 4.43 MHz synthesis clock. Frequency Synthesizer 4*Fsc for 4.43361875 MHz. (For REG_FSC_TABLE[4]=0.) Syncthesis-base/(4*Fsc)*2^22/8.	
81h	**NCO_FSC0**	**7:0**	**Default : 0x2D**	**Access : R/W**

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	FSC_NCO0[15:8]	7:0	{NCO_FSC0} 4.43 MHz synthesis clock.	
82h	**NCO_FSC0**	**7:0**	**Default : 0x01**	**Access : R/W**
	FSC_NCO0[7:0]	7:0	{NCO_FSC0} 4.43 MHz synthesis clock.	
83h	**NCO_FSC1**	**7:0**	**Default : 0x59**	**Access : R/W**
	FSC_NCO1[23:16]	7:0	Frequency synthesizer 4*Fsc for 3.57954545 MHz (For FSC_TABLE[4]=0).	
84h	**NCO_FSC1**	**7:0**	**Default : 0x65**	**Access : R/W**
	FSC_NCO1[15:8]	7:0	{NCO_FSC1} 3.579 MHz synthesis clock.	
85h	**NCO_FSC1**	**7:0**	**Default : 0x97**	**Access : R/W**
	FSC_NCO1[7:0]	7:0	{NCO_FSC1} 3.579 MHz synthesis clock.	
86h	**NCO_FSC2**	**7:0**	**Default : 0x59**	**Access : R/W**
	FSC_NCO2[23:16]	7:0	Frequency Syncthesizer 4*Fsc for 3.57561149 MHz (For FSC_TABLE[4] =0).	
87h	**NCO_FSC2**	**7:0**	**Default : 0x7E**	**Access : R/W**
	FSC_NCO2[15:8]	7:0	{NCO_FSC2} 3.582 MHz synthesis clock.	
88h	**NCO_FSC2**	**7:0**	**Default : 0x74**	**Access : R/W**
	FSC_NCO2[7:0]	7:0	{NCO_FSC2} 3.582 MHz synthesis clock.	
89h	**NCO_FSC3**	**7:0**	**Default : 0x59**	**Access : R/W**
	FSC_NCO3[23:16]	7:0	Frequency Sunthesizer 4*Fsc for 3.58205625 MHz (For FSC_TABLE[4] = 0).	
8Ah	**NCO_FSC3**	**7:0**	**Default : 0x55**	**Access : R/W**
	FSC_NCO3[15:8]	7:0	{NCO_FSC3} 3.576 MHz synthesis clock.	
8Bh	**NCO_FSC3**	**7:0**	**Default : 0x8B**	**Access : R/W**
	FSC_NCO3[7:0]	7:0	{NCO_FSC3} 3.576 MHz synthesis clock.	
8Ch	**REG_FSC_NCO4**	**7:0**	**Default : 0x4A**	**Access : R/W**
	FSC_NCO4[23:16]	7:0	Requency Synthesizer 4*Fsc for 4.28515625 MHz (For REG_FSC_TABLE[4] = 0).	
8Dh	**FSC_NCO4**	**7:0**	**Default : 0xAD**	**Access : R/W**
	FSC_NCO4[15:8]	7:0	Requency Synthesizer 4*Fsc for 4.28515625 MHz (For REG_FSC_TABLE[4] = 0).	
8Eh	**FSC_NCO4**	**7:0**	**Default : 0x27**	**Access : R/W**
	FSC_NCO4[7:0]	7:0	Requency Synthesizer 4*Fsc for 4.28515625 MHz (For REG_FSC_TABLE[4] = 0).	
8Fh	**FSC_TABLE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FSC_TABLE[4]	4	Frequency Synthesizer Control. 0: FSC_NCO0, 1, 2, 3, and 4 are used. 1: Specified by FSC_TABLE[3:2].	

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	FSC_TABLE[3:2]	3:2	Frequency Synthesizer Base. 00: 160MHz. 01: 15*14.31818MHz. 10: 216MHz. 11: 15*14.31818MHz. Only valid for FSC_TABLE[4] =1.	
	FSC_TABLE[1:0]	1:0	Frequency Synthesizer Output. 00: 4*FSC. 01: 8*FSC. 10: 16*FSC. 11: 16*FSC.	
90h	**FSC_NCO_ERR_443**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSC_NCO_ERR_443 [15:8]	7:0	Frequency Synthesizer 4*Fsc Error for 4.43MHz; 2's Complement (Auto scaled internally for 3.58MHz).	
91h	**FSC_NCO_ERR_443**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSC_NCO_ERR_443 [7:0]	7:0	Frequency Synthesizer 4*Fsc Error for 4.43MHz; 2's Complement (Auto scaled internally for 3.58MHz).	
92h	**WINIIR_THRD_CTRL**	**7:0**	**Default : 0xA7**	**Access : R/W**
	WINIIR_THRD1	7:4	IIR Window Threshold 1.	
	WINIIR_THRD0	3:0	IIR Window Threshold 0.	
93h	**WINFIR_THRD_CTRL**	**7:0**	**Default : 0xA4**	**Access : R/W**
	WINFIR_THRD1	7:4	IIR Window Threshold 1.	
	WINFIR_THRD0	3:0	IIR Window Threshold 0.	
94h	**SPL_SPD_CTRL1**	**7:0**	**Default : 0x14**	**Access : R/W**
	SPL_SPD_FORCE	7:5	Coarse HSYNC PLL Tracking Speed. Bit[2] forces using Bit[1:0]. SPL_SPD=3: Fastest. SPL_SPD=0: Slowest.	
	SPL_SPD_SRCH	4:3	Coarse HSYNC PLL tracking Speed during HSYNC-Search.	
	SPL_SPD_CLEAN	2:1	Coarse HSYNC PLL tracking Speed for Clean signal.	
	-	0	Reserved.	
95h	**SPL_SPD_CTRL2**	**7:0**	**Default : 0x2A**	**Access : R/W**
	SPL_SPD_NOISY	7:6	Coarse HSYNC PLL tracking Speed for Noisy signal.	
	SPL_SPD_VCR	5:4	Coarse HSYNC PLL phase tracking Speed for VCR outside VSYNC.	
	SPL_SPD_VCR_V	3:2	Coarse HSYNC PLL Phase Tracking Speed for VCR during VSYNC.	
	SPL_SPD_VCR_PRE	1:0	Coarse HSYNC PLL HSYNC-search lines. 00: 48. 01: 64. 10: 80. 11: 96.	
96h	**EDGES_NOISY_THRD**	**7:0**	**Default : 0xA0**	**Access : R/W**

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	NOISE_DC_SEL	7:6	Noise magnitude estimation DC level Selection. 00: IIR_8. 01: IIR_8. 10: CCTRAP_13. 11: CCTRAP.	
	EDGES_NOISY	5:0	Threshold of the average number of sliced Edges per Line to determine Noisy mode (/ 4).	
97h	**EDGES_CLEAN_THRD**	**7:0**	**Default : 0x05**	**Access : R/W**
	SYNC_INMUX[2:1]	7:6	Slicer input pre-filter selection. 00: CCTRAP. 01: CCTRAP_13. 10: IIR_8. 11: IIR_16.	
	SYNC_INMUX[0]	5	Slicer Auxiliary Pre-Filter Selection. 0: IIR_8. 1: IIR_16.	
	-	4	Reserved.	
	EDGES_CLEAN	3:0	Threshold of the average number of sliced Edges per line to determine Clean mode (/ 4).	
98h	**SYNC_WIN_CTRL1**	**7:0**	**Default : 0x43**	**Access : R/W**
	SYNC_INMUX_VCR [2:0]	7:5	HSYNC slicer Input selection.	
	-	4	Reserved.	
	WIN_NOISY	3:0	Ciarse HSYNC PLL PD Limitaion Window Width for Noisy Mode (*8+7).	
99h	**SYNC_WIN_CTRL2**	**7:0**	**Default : 0x88**	**Access : R/W**
	SYNC_WIN	7:4	Coarse HSYNC PLL SYNC-lost detection Window width (*4+4).	
	SYNC_WIN_SRCH	3:0	Coarse HSYNC PLL SYNC-found detection Window width (*4+4).	
9Ah	**SYNC_CTRL1**	**7:0**	**Default : 0xF0**	**Access : R/W**
	SYNC_THRD_MISS	7:4	Coarse HSYNC PLL SYNC search fail Threshold.	
	-	3:2	Reserved.	
	SPL_SRCH_LENG	1:0	SPL Search Length.	
9Bh	**SYNC_CTRL2**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	SYNC_THRD	5:0	Coarse HSYNC PLL SYNC search pass (SYNC Found) Threshold (*4+3).	
9Ch	**SYNC_CTRL3**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7	Reserved.	
	SYNC_THRD_LOST	6:0	Coarse HSYNC PLL SYNC SYNC-Lost Threshold (*16+15).	
9Dh	**DPL_NSPL_HIGH**	**7:0**	**Default : 0x6C**	**Access : R/W**

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	DPL_NSPL[10:3]	7:0	PI-Type Display PLL Number of Samples per Line (MSB); typically 864.	
9Eh	**DPL_NSPL_LOW**	**7:0**	**Default : 0x00**	**Access : R/W**
	DPL_NSPL[2:0]	7:5	PI-type Display PLL Number of Samples per Line (LSB); typically 864.	
	DPLL_TRUE8FSC	4	DPLL under 8 Fsc mode.	
	-	3:0	Reserved.	
9Fh	**SPL_K2_VCR**	**7:0**	**Default : 0x40**	**Access : R/W**
	SPL_K2_VCR	7:6	Coarse HSYNC PLL Frequency Tracking Speed for VCR.	
	SPL_NSPL_LMT	5:0	PI-type display PLL frequency coasts if the coarse HSYNC PLL deviation is larger than +/- 4*SPL_NSPL_LMT (Try).	
A0h	**DPL_K1_FORCE**	**7:0**	**Default : 0x20**	**Access : R/W**
	DPL_K_FORCE	7	Force DPL K value.	
	-	6	Reserved.	
	DPL_K1	5:0	PI-type Display PLL phase tracking coefficient K1.	
A1h	**DPL_K2_FORCE**	**7:0**	**Default : 0x60**	**Access : R/W**
	DPL_K2	7:0	PI-type Display PLL frequency tracking coefficient K2.	
A2h	**DPL_K1_NOISY**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	DPL_K1_NOISY	5:0	PI-type Display PLL phase tracking coefficient for Noisy broadcast.	
A3h	**DPL_K2_NOISY**	**7:0**	**Default : 0x04**	**Access : R/W**
	DPL_K2_NOISY	7:0	PI-type Display PLL frequency tracking coefficient for Noisy broadcast.	
A4h	**DPL_K1_VCR**	**7:0**	**Default : 0x34**	**Access : R/W**
	-	7:6	Reserved.	
	DPL_K1_VCR	5:0	PI-type Display PLL phase tracking coefficient for VCR.	
A5h	**DPL_K2_VCR**	**7:0**	**Default : 0x6A**	**Access : R/W**
	DPL_K2_VCR	7:0	PI-type Display PLL frequency tracking coefficient for VCR.	
A6h	**DPL_K1_VCR_V**	**7:0**	**Default : 0x34**	**Access : R/W**
	-	7:6	Reserved.	
	DPL_K1_VCR_V	5:0	PI-type Display PLL phase tracking coefficient for VCR during VSYNC.	
A7h	**DPL_K2_VCR**	**7:0**	**Default : 0x2C**	**Access : R/W**
	-	7:6	Reserved.	
	DPL_VCR_FADE_SPD	5:4	PI-type Display PLL PD_MAX fading speed from VSYNC to active lines. 00: Slow. 11: Fast.	
	DPL_VCR_FADE_START	3:0	PI-type Display PLL PE_MAX fading Start lines (*2).	
A8h	**DPL_K1_FAST**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	DPL_K1_FAST	5:0	PI-type Display PLL phase tracking coefficient for Fast mode and initialization.	
A9h	**DPL_K2_FAST**	**7:0**	**Default : 0x65**	**Access : R/W**
	DPL_K2_FAST	7:0	PI-type Display PLL frequency tracking coefficient for Fast mode and initialization.	
AAh	**DPL_CTRL1**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	DPL_FAST_LINES	3:0	PI-type Display PLL Fast Mode Lines. (*256)	
ABh	**DPL_PD_MAX**	**7:0**	**Default : 0x10**	**Access : R/W**
	DPL_PD_MAX	7:0	PI-type Display PLL Phase Detector (DPL_PD) Limit. If bit[7]=1, force using bit[6:0].	
ACh	**DPL_PD_MAX_VCR**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DPL_PD_MAX_VCR	7:0	PI-type Display PLL phase detector (DPL_PD) limit for VCR ouside VSYNC area.	
ADh	**REG_656_CTRL**	**7:0**	**Default : 0x3A**	**Access : R/W**
	REG_656_OPTION1	7	Line Middle Method 0 Selection.	
	REG_656_OPTION0	6	Line Middle Method 1 Selection.	
	REG_DPL_WAIT_LENG	5:4	DPL Wait Length.	
	REG_DPL_NCO_RST	3	DPL NCO Reset enable.	
	DPL_FAST_RE_DO	2	PI-type Display PLL Re-Do Fast Mode.	
	DPL_NO_STOP	1	PI-type Display PLL Never Stops. (Free Run when HSYNC not found.)	
	DPL_COAST_T_FORCE	0	PI-type Display PLL Frequency Frozen Always. (except when Fast Mode and Initialization)	
AEh	**DPL_COAST_CTRL**	**7:0**	**Default : 0xB8**	**Access : R/W**
	VSYNC_SEL	7	VSYNC source Selection.	
	-	6	Reserved.	
	COAST_V_ALWAYS	5	Always V Coast function.	
	DPL_COAST_T_LINES	4:0	Lines where 656 PLL coast frequency during V. PI-type Display PLL Frequency Frozen Lines during VSYNC. (*2)	
AFh	**DPL_CTRL2**	**7:0**	**Default : 0x85**	**Access : R/W**
	DPL_LOST_LINES	7:4	PI-type Dislay PLL Threshold on Lines to Determine Out-of –Lock. (*64).	
	DPL_LOST_WIN	3:0	PI-type Display PLL HSYNC Window Width to Detect Out-of-Lock. (*8)	
B0h	**DPL_K1_FREE**	**7:0**	**Default : 0x86**	**Access : R/W**
	DPL_K1_FREE	7:4	PI-type Dipslay PLL Phase Tracking Coefficient during HSYNC not found.	
	BKPRH_JUMP_MAX	3:0	Back-Porch-Jump Maximal Lines. (Try.) (Can move to SW Clmp.)	
B1h	**BKPRH_JUMP_CTRL**	**7:0**	**Default : 0x06**	**Access : R/W**

Video Decoder Register (Bank = 02)

Index	Name	Bits	Description	
	-	7	Reserved.	
	BKPRH_JUMP_MV_EN	6:5	Back-Porch-Jump used to Pause Clamping when Macrovision found (if set 01). (Try.) (Can move to SW Clmp.)	
	BKPRH_JUMP_THRD	4:0	Back-Porch-Jump Threshold. (*32+32). (Try.) (Can move to SW Clmp.)	
B2h	**SPL_DELAY_FIR**	**7:0**	**Default : 0x19**	**Access : R/W**
	-	7:6	Reserved.	
	SPL_DELAY_FIR	5:0	Coarse HSYNC PLL Delay with Respect to the Actual HSYNC Leading Edge if SYNC_INMUX selects CCTRAP or CCTRAP_13.	
B3h	**SPL_DELAY_IIR**	**7:0**	**Default : 0x1E**	**Access : R/W**
	-	7	Reserved.	
	SPL_DELAY_IIR	6:0	Coarse HSYNC PLL Delay with Respect to the Actual HSYNC Leading Edge if SYNC_INMUX selects IIR_8 or IIR_16.	
B4h	**REG_PB_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	REG_PB_EN	7	0: Hold ADC Data Probe. 1: Enable ADC Data Probe.	
	REG_PB_4FSC	6	0: Probe 8Fsc ADC Data when 8Fsc Clock. 1: Probe 4Fsc ADC Data when 8Fsc Clock.	
	REG_PB_LINE	5:4	1: Probe ADC Data in Next Line.	
	REG_PB_YC	3	0: Probe Y(CBVS) ADC Data. 1: Probe C ADC Data.	
	REG_PB_10B	2	0: Probe 8 bit Data. 1: Probe 10 bit Data.	
	-	1:0	Reserved.	
B5h	**PROBE_OUT**	**7:0**	**Default : 0x00**	**Access : R**
	PROBE_OUT	7:0	ADC Probe Data. (RP_LSB) ? {6'b0, PROBE_OUT1[1:0]} : PROBE_OUT1[9:2].	
B6h	**REG_PB_HPOS**	**7:0**	**Default : 0x00**	**Access : R/W**
	REG_PB_HPOS[7:0]	7:0	Start Probe Horizontal Position. (lower 8 bits)	
B7h	**REG_PB_BPOS1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	REG_PB_VPOS[10:8]	5:4	Start Probe Vertical Position. (upper 3 bits)	
	REG_PB_HPOS[10:8]	2:0	Start Probe Horizontal Position. (upper 3 bits)	
B8h	**REG_PB_VPOS2**	**7:0**	**Default : 0x00**	**Access : R/W**
	REG_PB_VPOS[7:0]	7:0	Start Probe Vertical Position. (lower 8 bits)	
B9h	**REG_WP_HOVER THRD**	**7:0**	**Default : 0x1F**	**Access : R/W**
	REG_WP_HOVER THRD[7:0]	7:0	Overflow Threshold of ADC Value.	

Video Decoder Register (Bank = 02)				
Index	**Name**	**Bits**	**Description**	
BAh	**REG_WP_HUNDERTHRD**	**7:0**	**Default : 0x1F**	**Access : R/W**
	REG_WP_HUNDERTHRD[7:0]	7:0	Underflow Threshold of ADC Value.	
BBh ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

Comb-Filter Register (Bank = 03, Registers 01h ~ 9Fh)

Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)				
Index	**Name**	**Bits**	**Description**	
00h ~ 09h	**-**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:0	Reserved.	
10h	**COMBCFGA**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7	Reserved.	
	SVDOCBP	6	Band Pass Filter for S-Video C Channel to kill the DC Level.	
	DIRADCIN	5	Direct use ADC Input (Bypass AFEC).	
	DDETSRCSEL	4	Degree Detect Source Select. 0: Without ACC. 1: After ACC.	
	MANUCOMB	3	0: Auto Select Working Mode. 1: Manual Select Working Mode.	
	WORKMD	2:0	Working Mode. 000: Off. 001: Notch. 010: 2D Comb. 011: 3D Comb. 100: 3D Comb with History.	
11h	**COMBCFGB**	**7:0**	**Default : 0x00**	**Access : R/W**
	FORCE8BIT	7	Force 8 bit.	
	GOODHS	6	Using Free Run HSYNC in Standard Input.	
	AFEC_DEM	5	Select AFEC Demodulation.	
	PALCMINV	4	PalCmpUp Inverse.	
	-	3	Reserved.	
	SYNCONY	2	SYNC on Y.	
	CRMA_OFF	1	Turn Off the Chroma of video decoder output. 0: Normal. 1: Off.	
	BST_OFF	0	Turn Off the Color Burst of video decoder output. 0: Normal. 1: Off.	
12h	**COMBCFGC**	**7:0**	**Default : 0x10**	**Access : R/W**
	FREESYNC	7	H/V SYNC Free Run.	

Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	FREECNTMD	6	Free Run Counter Mode. 0: NTSC. 1: PAL.	
	SNOWTYPE	5:4	Snow Type. 00: Never snow. 01: Snow when VDOMD = 7. 10, 11: Force snow.	
	RND_MD	3:2	Rounding Mode. 00: Truncate. 01: Rounding. 10: Dithering. 11: Error Feedback.	
	-	1:0	Reserved.	
13h	**YGAIN**	**7:0**	**Default : 0xC8**	**Access : R/W**
	YGAIN	7:0	Luma Gain for U/V Demodulation. Out=In*Gain+16. 0: 0. 128: 1. 255: 1.992.	
14h	**CBGAIN**	**7:0**	**Default : 0x96**	**Access : R/W**
	CBGAIN	7:0	Cb Gain for U/V Demodulation.	
15h	**CRGAIN**	**7:0**	**Default : 0x6A**	**Access : R/W**
	CRGAIN	7:0	Cr Gain for U/V Demodulation.	
16h	**DITHCTRLA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CTSTDITHEN	6	Dithering when Contrast Adjustment.	
	CTSTDITHPOS	5:4	Dithering Position (Offset) of Contrast.	
	-	3	Reserved.	
	SATDITHEN	2	Dithering when Saturation Adjustment.	
	SATDITHPOS	1:0	Dithering Position (Offset) of Saturation.	
17h	**DITHCTRLB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDEMDITHEN	6	Dithering when Demodulation Y-Gain.	
	YDEMDITHPOS	5:4	Dithering Position (Offset) of Y Gain.	
	-	3	Reserved.	
	CDEMDITHEN	2	Dithering when Demodulation C-Gain.	
	CDEMDITHPOS	1:0	Dithering Position (Offset) of C Gain.	
18h	**HORSTPOS**	**7:0**	**Default : 0xC0**	**Access : R/W**
	HORSTPOS[7:0]	7:0	Horizontal Starting Position. 0..255 : -128..127.	
19h	**FRHTOTL**	**7:0**	**Default : 0x8D**	**Access : R/W**
	FRHTOTL	7:0	Free Run HSYNC Total Low Byte.	

Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
1Ah	**FRHTOTH**	**7:0**	**Default : 0x03**	**Access : R/W**
	FRHTOTH	7:0	Free Run HSYNC Total High Byte.	
1Bh	**PHSDETCFG**	**7:0**	**Default : 0x83**	**Access : R/W**
	PHSDETEN	7	Line-Lock Phase Detection Enable.	
	PHSDETINV	6	Output Inverse.	
	-	5:3	Reserved.	
	PHSDETSFT	2:0	Shift Bit Number. 000: Only output integer. 001: Output shift right 1 bit. … 111: Output shift right 7 bit.	
	CTRLSWCH	**7:0**	**Default : 0xF0**	**Access : R/W**
	HSFRAFEC	7	H-SYNC from AFEC.	
	VSFRAFEC	6	V-SYNC from AFEC.	
	BLKFRAFEC	5	Black Level from AFEC.	
	DEGFRAFEC	4	Demodulation Degree from AFEC.	
	-	3:2	Reserved.	
	STDSEL	1:0	NTSC/PAL Decision. 01: force NTSC. 10: force PAL. Other: Auto detect.	
20h	**COMB2DCFGA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:0	Reserved.	
21h	**COMB2DCFGB**	**7:0**	**Default : 0xD4**	**Access : R/W**
	CRMATRP_EN	7	C-Trap of C Enable.	
	NCHMD_Y[2:0]	6:4	Notch Mode of Y.	
	CHRMFLT_EN	3	Chroma Median Filter Enable. 0: Off 1: Enable	
	NCHMD_C[2:0]	2:0	Notch Mode of C.	
22h	**COMB2DCFGC**	**7:0**	**Default : 0x83**	**Access : R/W**
	LNENDPOS	7:4	Line End Offset. 0~15: -8~7.	
	SHARP2DMD	3:2	Sharpness Mode of 2D Comb. 00: Off. 01: Mode 1. 10: Mode 2. 11: Mode 3.	
	CDEMCHK	1	Chroma Vertical Check (dem).	
	FORCE5LN	0	Force use 5 Line even in 1D.	
23h	**HDYGAIN**	**7:0**	**Default : 0x40**	**Access : R/W**
	HDYGAIN	7:0	Gain of Chroma Trap for Hanging Dots.	
24h	**HDCGAIN**	**7:0**	**Default : 0x20**	**Access : R/W**

Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	HDCGAIN	7:0	Gain of Chroma Trap for Hanging Dots.	
25h	**ETPREF**	**7:0**	**Default : 0x18**	**Access : R/W**
	ETPREF	7:0	Gain of Chroma Trap for Hanging Dots.	
26h	**ETPTHH**	**7:0**	**Default : 0x00**	**Access : R/W**
	ETPTHH	7:0	Horizontal Entropy Threshold for Chroma Trap in 2D Comb.	
27h	**ETPTHV**	**7:0**	**Default : 0x00**	**Access : R/W**
	ETPTHV	7:0	Vertical Entropy Threshold for Chroma Trap in 2D Comb.	
28h	**THDEM**	**7:0**	**Default : 0x10**	**Access : R/W**
	THDEM	7:0	Thresholds for 2D Comb Filter; check separated chroma complement with up/down line or not.	
29h ~ 2Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
2Fh	**IFCOEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	IFCOEF	7:0	If compensation Coefficient. 2-bit integer, 6-bit fraction. Crma=C_cn–(Coef*(C_left+C_right)).	
30h ~ 3Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
40h	**HVDETCFG**	**7:0**	**Default : 0x80**	**Access : R/W**
	SENSSYNCLVL	7:5	Sensitivity of SYNC Level Detect.	
	-	4:3	Reserved.	
	BLNKDETMD	2	Blank Level Detect Mode. 0: Either 240 or 252. 1: 230~262 is possible.	
	VDETMD	1:0	Vertical Timing Detect Mode. 00, 01: Auto detect. 10: force 525 line system. 11: force 625 line system.	
41h	**SENSSIGDET**	**7:0**	**Default : 0x08**	**Access : R/W**
	SENSSIGDET	7:0	Sensitivity of Signal Detect.	
42h	**SYNCLVLTLRN**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SYNCLVLTLRN	7:0	SYNC Level Tolerance.	
43h	**VCRCOASTLEN**	**7:0**	**Default : 0x60**	**Access : R/W**
	VCRCOASTLEN	7:0	VCR Coast Length.	
44h	**REGHBIDLY**	**7:0**	**Default : 0x80**	**Access : R/W**
	REGHBIDLY	7:0	Horizontal Blanking Region Delay. 0 … 255 : Delay -128 .. 127 pixels.	
45h ~ 47h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
48h	**DEGDETCFG**	**7:0**	**Default : 0x00**	**Access : R/W**
	YCPIPE	7:6	Y/C Pipe Delay.	

Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	DEGPIPE	5:4	Degree Pipe Delay.	
	DEG1LNMD	3	Using just one line's Burst Determine the Degree.	
	DEGSENS	2:0	Sensitivity of Degree Detect. 000: Directly use AFEC degree. 001: Tolerate 16384 errors. 010: Tolerate 8192 errors. 011: Tolerate 4096 errors. 100: Tolerate 2048 errors. 101: Tolerate 1024 errors. 110: Tolerate 512 errors. 111: Tolerate 256 errors.	
49h	**THBURST**	**7:0**	**Default : 0x1E**	**Access : R/W**
	THBURST	7:0	Degree Detection Tolerance Registers.	
4Ah	**TLRNSWCHERR**	**7:0**	**Default : 0xC8**	**Access : R/W**
	TLRNSWCHERR	7:0	Degree Detection Tolerance Registers.	
4Bh	**HSLEADRGN**	**7:0**	**Default : 0x80**	**Access : R/W**
	HSLEADRGN	7:0	HSYNC Leading Edge Range, for Even/Odd Detect.	
4Ch ~ 4Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
50h	**TIMDETCFGA**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	AUTOSTOPSYNC	3	Automatic Stop H/V Sync when No Input.	
	LNFREEMD	2:0	Line Buffer Free Run Mode. 000: Off (always synchronize). 001: 909 return. 010: 910 return. 011: 917 return. 100: 1127 return. 101: 1135 return. 110: Decided by register. 111: Automatic.	
51h	**TIMDETCFGB**	**7:0**	**Default : 0x00**	**Access : R/W**
	STBCNTMD	7:6	Stable Counter Mode. 00: div 16. 01: div 32. 10: div 64. 11: div 128.	
	HSSTBDEC	5:0	HSYNC Stable Counter Decrease Speed.	
52h	**HRETPOSL**	**7:0**	**Default : 0x8E**	**Access : R/W**
	HRETPOSL	7:0	Horizontal Return Position in Line Buffer Free Run Mode.	
53h	**HRETPOSH**	**7:0**	**Default : 0x03**	**Access : R/W**
	HRETPOSH	7:0	Horizontal Return Position in Line Buffer Free Run Mode.	
54h	**TILTTLRN**	**7:0**	**Default : 0x02**	**Access : R/W**
	TILTTLRN	7:0	Line Position Tilt Tolerance.	

Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
55h	**JITTLRN3D**	**7:0**	**Default : 0x08**	**Access : R/W**
	JITTLRN3D	7:0	3D Timing Detection Tolerance.	
56h	**LCKSTEP**	**7:0**	**Default : 0x80**	**Access : R/W**
	LCKSTEP	7:0	3D Lock Counter Go Back Distance when SYNC Unstable.	
57h	**LCK3DTHU**	**7:0**	**Default : 0x33**	**Access : R/W**
	LCK3DTHU	7:0	3D Timing Detection Threshold.	
58h	**LCK3DTHL**	**7:0**	**Default : 0x11**	**Access : R/W**
	LCK3DTHL	7:0	3D Timing Detection Threshold.	
59h	**JITTLRN1**	**7:0**	**Default : 0x08**	**Access : R/W**
	JITTLRN1	7:0	Tolerance of H-SYNC Jitter.	
5Ah	**JITTLRN2**	**7:0**	**Default : 0x20**	**Access : R/W**
	JITTLRN2	7:0	Tolerance of H-SYNC Jitter.	
5Bh	**HSLCKTHU**	**7:0**	**Default : 0x10**	**Access : R/W**
	HSLCKTHU	7:0	Upper Bound Threshold of Hysteresis H-SYNC Lock Counter.	
5Ch	**HSLCKTHL**	**7:0**	**Default : 0x08**	**Access : R/W**
	HSLCKTHL	7:0	Lower Bound Threshold of Hysteresis H-SYNC Lock Counter.	
5Dh	**HSCHGTLRN**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HSCHGTLRN	7:0	Tolerance of HSYNC Counter Change Times. Even HSYNC locked, but if timing drifted too many times, systme still should turn off 2D/3D. 00h: immediately stop 2D/3D when HsChg happen. FFh: Never stop 2D/3D if HsLock.	
5Eh	**SYNCDLY**	**7:0**	**Default : 0x14**	**Access : R/W**
	SYNCDLY	7:0	H SYNC (from Decoder to Scaler) Pipe Delay.	
5Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
60h	**IMGCTRL**	**7:0**	**Default : 0xF0**	**Access : R/W**
	COLKILLMD	7:6	Color Kill Mode. 00: Off. 01: Auto. 10, 11: Decided by MCU.	
	CGMODE	5:4	Auto Chroma Gain Mode. 00: Off. 01: Auto. 10, 11: Manual.	
	AC_MD	3	Auto Contrast Mode. 0: Double at most. 1: 4 times at most.	
	AUTO_CSTS	2	Auto Contrast Adjustment.	
	-	1	Reserved.	
	AUTO_SAT	0	Auto Saturation Adjustment.	
61h	**RSPNTIME**	**7:0**	**Default : 0x10**	**Access : R/W**

Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	RSPNTIME	7:0	Response Time of Contrast/Brightness Adjust. 0… 255 => 1… 256 field.	
62h	**REGBSTHGHT**	**7:0**	**Default : 0x00**	**Access : R/W**
	REGBSTHGHT	7:0	Burst Height for Auto Chroma Gain. 0: Auto, 112 for NTSC and 117 for PAL. Other: use RegBstHght/DetBstHght as C Gain.	
63h	**REGCTST**	**7:0**	**Default : 0x80**	**Access : R/W**
	REGCTST	7:0	Contrast adjustment Coefficient. 0… 255 => 0… (255/128).	
64h	**REGBRHT**	**7:0**	**Default : 0x80**	**Access : R/W**
	REGBRHT	7:0	Brightness adjustment Coefficient. 0… 255 => -128… 127 in 8-bit precision.	
65h	**REGSAT**	**7:0**	**Default : 0x80**	**Access : R/W**
	REGSAT	7:0	Saturation adjustment Coefficient. 0… 255 => (0… 255)/128.	
66h	**CKTHU**	**7:0**	**Default : 0x80**	**Access : R/W**
	CKTHU	7:0	Upper Bound Threshold of Color Kill.	
67h	**CKTHL**	**7:0**	**Default : 0x30**	**Access : R/W**
	CKTHL	7:0	Lower Bound Threshold of Color Kill.	
68h	**CRMAGAINL**	**7:0**	**Default : 0x80**	**Access : R/W**
	CRMAGAINL	7:0	Chroma Gain Value for Manu Chroma Gain.	
69h	**CRMAGAINH**	**7:0**	**Default : 0x00**	**Access : R/W**
	CRMAGAINH	7:0	Chroma Gain Value for Manu Chroma Gain.	
6Ah	**MAXLUMA**	**7:0**	**Default : 0xB0**	**Access : R/W**
	MACLUMA	7:0	Max Luminance for Auto Contrast Adjust.	
6Bh	**MAXSAT**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MAXSAT	7:0	MAX Saturation for Auto Saturation Adjust.	
6Ch	**MAXCRMA**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MAXCRMA	7:0	MAX Chrominance for Auto Saturation Adjust.	
6Dh	**SNOWDELAY**	**7:0**	**Default : 0x80**	**Access : R/W**
	SNOWDELAY	7:0	Latency of Snow Output after Signal Missing.	
6Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
6Fh	**CBCRLPCFG**	**7:0**	**Default : 0x04**	**Access : R/W**
	CTIIIRMD	7:6	IIR Coeficient for CTI. 00: 1/4. 01: 1/8. 10: 1/16. 11: 1/32.	

Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

Index	Name	Bits	Description	
	CTIMODE	5:4	CTI Mode. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
	YPIPDLY	3:2	Luma Pipe Delay. 00: -1 cycle. 01: 0 cycle. 10: 1 cycle. 11: 2 cycle.	
	CBCRLPMD	1:0	Cb/Cr Low Pass Mode. 0: Off. 01: Cut off at 2.0MHz. 10: Cut off at 1.5MHz. 11: Cut off at 1.0MHz	
70h	**COMBSTATUSA**	**7:0**	**Default : -**	**Access : Write one clear**
	HSLOCK	7	HSYNC Lock Happen.	
	LOCK3D	6	Good Timing (Lock3D) Happen.	
	-	5:4	Reserved.	
	HSLOCKZ	3	HSYNC Unlock Happen.	
	LOC3DZ	2	Good Timing (Lock3D) Disappear.	
	HSCHG	1	H-SYNC Counter Change.	
	-	0	Reserved.	
71h	**COMBSTATUSB**	**7:0**	**Default : -**	**Access : Write one clear**
	-	7:6	Reserved.	
	CCHNLACT	5	C-channel Active (maybe S-Video Input).	
	CCHNLACT	4	C-channel Quiet (maybe CVBS Input0.	
	-	3	Reserved.	
	FLDCNTCHG	2	Field Counter Change.	
	PALSWCHERR	1	PAL Switch Error.	
	DEGERR	0	Degree Error (Degree Detect).	
72h	**COMBSTATUSC**	**7:0**	**Default : -**	**Access : RO**
	LN525	7	525 Line System.	
	LN625	6	625 Line System.	
	F358	5	3.58 MHz System.	
	F443	4	4.43 MHz System.	
	NOINPUT	3	No Input.	

Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)				
Index	**Name**	**Bits**	**Description**	
	VDOMD	2:0	Video Mode. 000: NTSC(M). 001: NTSC(443). 010: PAL (M). 011: PAL(B,D,G,H,I,N). 100: PAL(Nc). 101: PAL(60). 110: Input without Burst. 111: Unknown.	
73h	**DETBLANKLVL**	**7:0**	**Default : -**	**Access : RO**
	DETBLANKLVL	7:0	Detected Blanking Level.	
74h	**CURBLANKLVL**	**7:0**	**Default : -**	**Access : RO**
	CURBLANKLVL	7:0	Detected Blanking Level.	
75h	**DETSYNCLVL**	**7:0**	**Default :-**	**Access : RO**
	DETSYNCLVL	7:0	Detected Sync Level.	
76h	**DETSYNCHGHT**	**7:0**	**Default : -**	**Access : RO**
	DETSYNCHGHT	7:0	Detected SYNC Height.	
77h	**DETBURSTHGHT**	**7:0**	**Default : -**	**Access : RO**
	DETBURSTHGHT	7:0	Detected Burst Level.	
78h	**DETHORTOTALL**	**7:0**	**Default : -**	**Access : RO**
	DETHORTOTALL	7:0		
79h	**DETHORTOTALH**	**7:0**	**Default : -**	**Access : R**
	DETHORTOTALH	7:0		
7Ah ~ 7Ch	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
7Dh	**COMBCTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMBCTRL	7:0	Some Control Signals for FPGA.	
7Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
7Fh	**FPGACTRL**	**7:0**	**Default : 0xE0**	**Access : R/W**
	FPGACTRL	7:0	Some Control Signals for FPGA.	
80h ~ 9Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

SECAM Register (Bank 03, Registers A0h ~ FFh)

SECAM Register (Bank=03, Registers A0h ~ FFh)				
Index	**Name**	**Bits**	**Description**	
A0h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
A1h	**SCM_IDSET1**	**7:0**	**Default : 0x02**	**Access : R/W**

SECAM Register (Bank=03, Registers A0h ~ FFh)

Index	Name	Bits	Description	
	RST_FLT	7	Filter Reset. Set to 1 to Reset the vaules of Filter Taps.	
	MIXC_EN	6	Chroma Mixing Enable. 0: Disable. 1: Enable.	
	WFUNC_ISO	5:4	Chroma Weighting Function Isolation.	
	SVEN	3	S-Video Input Enable. Set to 1 if the input is from S-Video interface.	
	ID_MODE	2	Identification Mode Selection. Set to 1 only if using frame ID for SECAM detection.	
	BS_TYPE	1	Band-Stop Filter TYPE. 0: Notch Dr Frequency. 1: Notch Db Frequency.	
	SCMID_EN	0	SECAM Identification Forced Enable. 0: Disbale. 1: Enable.	
A2h	**SAMPLE_START**	**7:0**	**Default : 0x90**	**Access : R/W**
	SAMPLE_ST[7:0]	7:0	Start of Sample Point (lower 8 bits).	
A3h	**SAMPLE_LENGTH**	**7:0**	**Default : 0x10**	**Access : R/W**
	SAMPLE_LEN	7:0	Length of Sample Numbers.	
A4h	**LINE_START_A**	**7:0**	**Default : 0x07**	**Access : R/W**
	LINE_STA	7:0	Start of Line Number of Odd Filed.	
A5h	**LINE_START_B**	**7:0**	**Default : 0x40**	**Access : R/W**
	LINE_STB[7:0]	7:0	Start of Line Number of Even Filed (lower 8 bits).	
A6h	**SCM_IDSET2**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7	Reserved.	
	SAMPLE_ST[10:8]	6:4	Start of Sample Point (upper 3 bits).	
	CMBGCLK_OPT	3	Comb Clock Gating Option. 0: Diable. 1: Enable ClkComb gating.	
	-	2	Reserved.	
	LINE_STB[9:8]	1:0	Start of Line Number of Even Filed (upper 2 bits).	
A7h	**LINE_LENGTH**	**7:0**	**Default : 0x02**	**Access : F/W**
	LINE_LEN	7:0	Length of Observation Line.	
A8h	**ACT_MULTIPLE**	**7:0**	**Default : 0x96**	**Access : R/W**
	ACT_MULTIPLE	7:0	Integer Multiple of LINE_LEN, combined to form Length of the Active Video Line.	
A9h	**MAG_THRSD_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAG_THRSD[7:0]	7:0	Magnitude Threshold (lower 8 bits).	
AAh	**MAG_THRSD_M**	**7:0**	**Default : 0x06**	**Access :**
	MAG_THRSD[15:8]	7:0	Magnitude Threshold (middle 8 bits).	
ABh	**MAG_THRSD_H**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	

SECAM Register (Bank=03, Registers A0h ~ FFh)

Index	Name	Bits	Description	
	LINE_PIXNUM[10:8]	6:4	Pixel Number of Line Buffer (upper 3 bits).	
	MAG_THRSD[19:16]	3:0	Magnitude Threshold (upper 4 bits).	
ACh	**LINE_PIXNUMBER**	**7:0**	**Default : 0x48**	**Access : R/W**
	LINE_PIXNUM[7:0]	7:0	Pixel Number of Line Buffer (lower 8 bits). (if the number is 1097, program 11'h448)	
ADh	**ID_THRSD**	**7:0**	**Default : 0x06**	**Access : R/W**
	ID_THRSD	7:0	Threshold for SECAM Identification.	
AEh	**SCM_THRSD**	**7:0**	**Default : 0x66**	**Access : R/W**
	NONSCM_THRSD	7:4	Non-SECAM Decision Threshold.	
	SCM_THRSD	3:0	SECAM Decision Threshold.	
AFh ~ CFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
D0h	**SCM_IDSTATUS**	**7:0**	**Default : -**	**Access : R**
	SCMID_DONE	7	SECAM Identification Done Indication.	
	SCMID_YES	6	SECAM Signal Found Bit.	
	DR_LINE	5	Dr Line Indication.	
	DB_LINE	4	Db Line Indication.	
	-	3	Reserved.	
	SCMID_STS	2:0	SECAM ID Status. 000: Idle 001, 010, 011: ID Progress 110: SECAM 111: No SECAM Signal Discovery	
D1h	**MAG_INT_L**	**7:0**	**Default : -**	**Access : R**
	MAG_INT[7:0]	7:0	Magnitude Accumulated Values for Observation (lower 8 bits).	
D2h	**MAG_INT_M**	**7:0**	**Default : -**	**Access : R**
	MAG_INT[15:8]	7:0	Magnitude Accumulated Values for Observation (middle 8 bits).	
D3h	**MAG_INT_H**	**7:0**	**Default : -**	**Access : R**
	MAG_INTB[19:16]	7:4	Magnitude Accumulated Values for Observation (upper 4 bits).	
	MAG_INT[19:16]	3:0	Magnitude Accumulated Values for Observation (upper 4 bits).	
D4h	**MAG_INT_B_L**	**7:0**	**Default : -**	**Access : R**
	MAG_INTB[7:0]	7:0	Magnitude Accumulated Values for Observation (lower 8 bits).	
D5h	**MAG_INT_B_M**	**7:0**	**Default : -**	**Access : R**
	MAG_INTB[15:8]	7:0	Magnitude Accumulated Values for Observation (meddle 8 bits).	
D6h	**SCM_FSC**	**7:0**	**Default : -**	**Access : R**
	-	7:2	Reserved.	
	SCM_FSC	1:0	Fsc Status from AFEC_TOP. 00: NTSC 3.58MHz 01: PAL 4.43MHz 10: SECAM 4.285156MHz	
D7h ~ F1h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

SECAM Register (Bank=03, Registers A0h ~ FFh)

Index	Name	Bits	Description	
F2h	**WR_LK1**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_LK1	7	Register Lock (work with WR_LK0). Register access is disabled when WR_LK0 and WR_LK1 are HIGH. Register access is enabled when WR_LK0 and WR_LK1 are LOW.	
	-	6:0	Reserved.	
F3h	**PWMCLK**	**7:0**	**Default : 0x00**	**Access : R/W**
	DB_EN	7	Double Buffer Enable. 0: Disable. 1: Enable.	
	P4REN	6	PWM4 Reset every frame Enable. 0: Disable. 1: Enable.	
	P3REN	5	PWM3 Reset every frame Enable. 0: Disable. 1: Enable.	
	P4POL	4	PWM 4 Polarity when enhance PWM4 enable.	
	EP4EN	3	Enhance PWM4 Enable. 0: Disable. 1: Enable.	
	P3POL	2	PWM3 Polarity when enhance PWM3 enable.	
	EP3EN	1	Enhance PWM3 Enable. 0: Disable. 1: Enable.	
	PCLK	0	PWM3/4 base Clock select. 0: 14.318MHz. 1: 14.318MHz / 4.	
F4h	**PWM3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM_14BIT_EN	7	14bit PWM Enable. 0: Disable, then PWM3C[6:0] = PWM3_CTUN[6:0]. 1: Enable, then PWM3C[3:0] = PWM_DIV.	
	PWM3_CTUN[6:0]	6:0	PWM3 Coarse adjustment, when PWM_14BIT_EN = 0.	
	-	6:4	Reserved.	
	PWM_DIV	3:0	Clock Divider, when PWM_14BIT_EN = 1.	
F5h	**PWM4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_POL	7	PWM4 Polarity.	
	PWM4_CTUN[6:0]	6:0	PWM4 Coarse adjustment.	
F6h	**PWM3EPL**	**7:0**	**Default : 0x00**	**Access : R/W**
	EPWM0P[7:0]	7:0	Enhance PWM3 Period, when PWM_14BIT_EN = 0.	
	PWM_FINE_TUNE	7:0	Fine Tune PWM Pulse, when PWM_14BIT_EN = 1.	
F7h	**PWM3EPH**	**7:0**	**Default : 0x00**	**Access : R/W**
	EPWM0P[15:8]	7:0	Enhance PWM3 Period, when PWM_14BIT_EN = 0.	
	PWM_MASK_BIT	5:0	Mask PWN Period Bits, when PWM_14BIT_EN = 1.	

SECAM Register (Bank=03, Registers A0h ~ FFh)				
Index	**Name**	**Bits**	**Description**	
F8h	**PWM4EPL**	**7:0**	**Default : 0x00**	**Access : R/W**
	EPWM4P[7:0]	7:0	Enhance PWM4 Period.	
F9h	**PWM4EPH**	**7:0**	**Default : 0x00**	**Access : R/W**
	EPWM4P[15:8]	7:0	Enhance PWM4 Period.	
FAh	**PWM3C_T**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	PWM3_POL	4	PWM3 Polarity.	
	-	3:0	Reserved.	
FBh ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

Embedded MCU Register (Address mapping from C000h to C0FFh)

Embedded MCU Register Bank – General Control Register				
Index	**Name**	**Bits**	**Description**	
00h ~ 07h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
08h	**WDT_KEY_L**	**7:0**	**Default : 0xAA**	**Access : R/W**
	WDT_KEY[7:0]	7:0	Watchdog timer disable key low byte Watchdog timer will be enabled If (WDT_Key_L != 8'hAA) or (WDT_Key_H != 8'h55)	
09h	**WDT_Key_H**	**7:0**	**Default : 0x55**	**Access : R/W**
	WDT_KEY[15:8]	7:0	Refer to C008h.	
0Ah	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
10h	**DDC2Bi_INT_EN**	**6:0**	**Default: 0x00**	**Access : R/W**
	START_EN	6	DDC2Bi Start interrupt Enable.	
	STOP_EN	5	DDC2Bi Stop interrupt Enable.	
	DATR_EN	4	DDC2Bi Data Reda interrupt Enable.	
	DATW_EN	3	DDC2Bi Data Write interrupt Enable.	
	DATRW_EN	2	DDC2Bi Data Read/Write interrupt Enable.	
	WADR	1	DDC2Bi Word Address interrupt.	
	ID	0	DDC2Bi ID interrupt.	
11h	**DDC2Bi_Flag**	**6:0**	**Default : 0x00**	**Access : R/C**
	DDC2Bi_FLAG		DDC 2Bi interrupt flag and clear	
12h	**DDC2Bi_W_BUF**	**7:0**	**Default : -**	**Access : RO**
			DDC2Bi write, MCU read buffer	
13h	**DDC2Bi_R_BUF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDC2Bi_R_BUF[7:0]	7:0	DDC2Bi read, MCU write buffer	
14h ~	**-**	**7:0**	**Default : -**	**Access : -**

Embedded MCU Register Bank – General Control Register

Index	Name	Bits	Description	
17h	-	7:0	Reserved.	
18h	**DDC2Bi_CTRL**	**1:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	EN_NO_ACK	1	DDC2Bi does not send ack if data buffer has not been read. 0: Disable. 1: Enable.	
	-	0	Reserved.	
19h	**DDC2Bi_ID**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDC2Bi_EN	7	DDC2Bi Enable.	
	DDC2Bi_ID[6:0]	6:0	DDCBi ID.	
1Ah ~ 1Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
20h	**KEY_ADC1**	**5:0**	**Default : -**	**Access : RO**
	KEY_ADC1[5:0]		Key Pad ADC channel 1 value.	
21h	**KEY_ADC2**	**5:0**	**Default : -**	**Access : RO**
	KEY_ADC2[5:0]		Key Pad ADC channel 2 value.	
22h	**KEY_ADC3**	**5:0**	**Default : -**	**Access : RO**
	KEY_ADC3[5:0]		Key Pad ADC channel 3 value.	
23h ~ 2Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
30h	**P0_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_CTRL[7:0]	7:0	MCU Port 0 output enable Control.	
31h	**P0_OE**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_OE[7:0]	7:0	MCU Port 0 Output Enable.	
32h	**P0_IN**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_IN[7:0]	7:0	MCU Port 0 output enable from output data.	
33h	**P1_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_CTRL[7:0]	7:0	MCU Port 1 output enable Control.	
34h	**P1_OE**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_OE[7:0]	7:0	MCU Port 1 Output Enable.	
35h	**P1_IN**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_IN[7:0]	7:0	MCU Port 1 output enable from output data.	
36h	**P2_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_CTRL[7:0]	7:0	MCU Port 2 output enable Control.	
37h	**P2_OE**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_OE[7:0]	7:0	MCU Port 2 Output Enable.	
38h	**P2_IN**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_IN[7:0]	7:0	MCU Port 2 output enable from output data.	
39h	**P3_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_CTRL[7:0]	7:0	MCU Port 3 output enable Control.	

Embedded MCU Register Bank – General Control Register

Index	Name	Bits	Description	
3Ah	**P3_OE**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_OE[7:0]	7:0	MCU Port 3 Output Enable.	
3Bh	**P3_IN**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_IN[7:0]	7:0	MCU Port 3 output enable from output data.	
3Ch	**P4_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	P4_CTRL[7:0]	7:0	MCU Port 4 output enable Control.	
3Dh	**P4_OE**	**7:0**	**Default : 0x00**	**Access : R/W**
	P4_OE[7:0]	7:0	MCU Port 4 Output Enable.	
3Eh	**P4_IN**	**7:0**	**Default : 0x00**	**Access : R/W**
	P4_IN[7:0]	7:0	MCU Port 4 output enable from output data.	
3Fh	**SSPI_STS_OP**	**7:0**	**Default : 0x05**	**Access : R/W**
	SPPI_STS_OP[7:0]	7:0	Soft-trigger SPI check status OP code.	
40h	**SSPI_WD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD0	7:0	Soft-trigger SPI Write byte 0.	
41h	**SSPI_WD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD1	7:0	Soft-trigger SPI Write byte 1.	
42h	**SSPI_WD2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD2	7:0	Soft-trigger SPI Write byte 2.	
43h	**SSPI_WD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD3	7:0	Soft-trigger SPI Write byte 3.	
44h	**SSPI_WD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD4	7:0	Soft-trigger SPI Write byte 4.	
45h	**SSPI_WD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD5	7:0	Soft-trigger SPI Write byte 5.	
46h	**SSPI_WD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD06	7:0	Soft-trigger SPI Write byte 6.	
47h	**SSPI_WD7**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_WD7	7:0	Soft-trigger SPI Write byte 7.	
48h	**SSPI_TRIG**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSPI_START	7	Trigger soft-SPI 0: NOP. 1: Start soft -SPI.	
	SSPI_CHK_BZY	6	Auto Check Busy after soft-SPI.	
	SSPI_CHK_BIT	5:3	Check busy bit position	
	SSPI_Length	2:0	SSPI command length.	
49h	**SSPI_RD1**	**7:0**	**Default : -**	**Access : RO**
	SSPI_RD1[7:0]	7:0	SSPI read byte 1.	
4Ah	**SSPI_RD2**	**7:0**	**Default : -**	**Access : RO**
	SSPI_RD2[7:0]	7:0	SSPI read byte21.	
4Bh	**SSPI_RD3**	**7:0**	**Default : -**	**Access : RO**

Embedded MCU Register Bank – General Control Register				
Index	**Name**	**Bits**	**Description**	
	SSPI_RD3[7:0]	7:0	SSPI read byte 3.	
4Ch	**SSPI_RD4**	**7:0**	**Default : -**	**Access : RO**
	SSPI_RD4[7:0]	7:0	SSPI read byte 4.	
4Dh	**SSPI_RD5**	**7:0**	**Default : -**	**Access : RO**
	SSPI_RD5[7:0]	7:0	SSPI read byte 5.	
4Eh	**SSPI_RD6**	**7:0**	**Default : -**	**Access : RO**
	SSPI_RD6[7:0]	7:0	SSPI read byte 6.	
4Fh	**SSPI_RD7**	**7:0**	**Default : -**	**Access : RO**
	SSPI_RD7[7:0]	7:0	SSPI read byte 7.	
50h	**ISP_PA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISP_PA[7:0]	7:0	Parallel flash ISP Address[7:0].	
51h	**ISP_PA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISP_PA[15:8]	7:0	Parallel flash ISP Address[15:8].	
52h	**ISP_PA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISP_PA[17:16]	7:0	Parallel flash ISP Address[17:16].	
53h	**ISP_PD_W**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISP_PD_W[7:0]	7:0	Parallel flash ISP Write Data.	
54h	**ISP_PCtr**	**4:0**	**Default : 0x0A**	**Access : R/W**
	ISP_PMD_EN	4	Parallel flash ISP mode enable.	
	ISP_PWEZ	3	Parallel flash WEZ at ISP mode.	
	ISP_POEZ	2	Parallel flash OEZ at ISP mode.	
	ISP_PDBUE	1	Parallel flash data bus output enable at ISP mode.	
	ISP_PCEZ	0	Parallel flash CEZ at ISP mode.	
55h	**ISP_PD_R**	**7:0**	**Default :-**	**Access : RO**
	ISP_PD_R[7:0]	7:0	Parallel flash ISP mode read data.	
56h ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
11/15/05		Created first version.

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